Designing Bang-Bang PLLs for Clock and Data Recovery in Serial Data Transmission Systems

Richard C. Walker

Abstract - **Clock recovery using phase-locked loops (PLL) with binary (bang-bang) or ternary-quantized phase detectors has become increasingly common starting with the advent of fully monolithic clock and data recovery (CDR) Circuits in the late 1980's. Bang-bang CDR circuits have the unique advantages of inherent sampling phase alignment, adaptability to multi-phase sampling structures, and operation at the highest speed at which a process can make a working flip-flop. This paper gives insight into the behavior of the nonlinear bang-bang PLL loop dynamics, giving approximate equations for loop jitter, recovered clock spectrum, and jitter tracking performance as a function of various design parameters. A novel analysis shows that the bang-bang loop output jitter grows as the square-root of the input jitter as contrasted with the linear dependence of the linear PLL.**

I. Introduction

Prior to the advent of fully monolithic designs, clock recovery was traditionally performed with some variant of the circuit in Fig. 1. The clock frequency component was typically extracted from

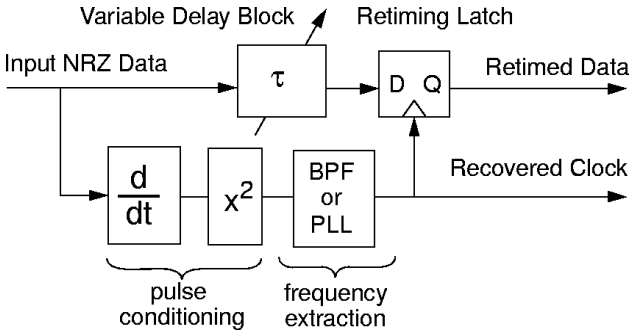

Fig. 1. Traditional non-monolithic clock and data recovery architecture.

the data stream using some combination of differentiation, rectification and filtering. The bandpass frequency filtering was provided by LC tank, surface acoustic wave (SAW) filter, dielectric resonator or PLL. Because the clock recovery path was separate from the data retiming path, it was difficult to maintain optimum sampling phase alignment over process, temperature, data-rate, and voltage variations. Even the PLL techniques had the drawback of using phase detectors with different set-up times than the retiming flip-flop so that the recovered clock was not intrinsically aligned to the optimum sampling point in the data eye. Circuits utilizing SAW resonator filtering typically required hand matching of SAW and circuit temperature coefficients along with custom cut coaxial delay lines for setting the timing of the recovered sampling clock with respect to the data eye [1].

Early monolithic CDR designs imitated these discrete block diagrams. The propagation delay differences between data and clock paths could be ignored as long as the gate delay skew was a negligible fraction of the total bit time, or unit interval. The need for higher link speeds grew faster than Moore's law, and as clock frequencies approached the effective f_T of the active devices, it became increasingly difficult to maintain an optimum sampling phase alignment between the recovered clock and the data over process, temperature, data-rate, and voltage variations.

A second problem was that most linear phase detectors produced narrow pulses with widths proportional to the phase error between the timing of the data and the clock [2], [3]. These narrow pulses required a process speed in excess of that required to simply sample data at a given rate. The timing skew and speed of linear phase detector circuits then became the limiting factor for aggressive designs.

Both these difficulties are eliminated by a family of circuits which simultaneously retime data and measure phase error by using matched flip-flops to sample both the middle of each data bit and the transitions between the data bits. Fig. 2 shows such an

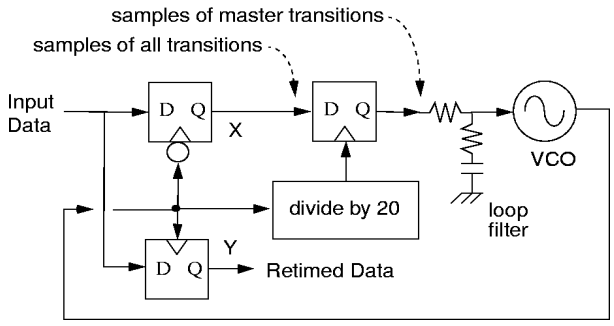

Fig. 2. A simple bang-bang loop using a flip-flop for a phase detector to lock onto a data stream with a guaranteed "0" to "1" transition every 20 bits.

early gigabit-rate monolithic example of such a circuit [4] which samples data with two matched flip-flops. Flip-flop "Y" samples the middle of each data bit on the rising edge of the VCO clock to produce retimed data, while flip-flop "X" samples the transition of each bit using the falling edge of the VCO clock.

The loop is designed to use the 16B/20B line code of Fig. 3 which guarantees a "01" "master transition" every 20 bits. The divide by 20 circuit and associated flip-flop in Fig. 2 discard every

R. Walker is with Agilent Laboratories, 3500 Deer Creek Road, MS 26-U4, Palo Alto CA 94304. (e-mail: rick_walker@labs.agilent.com).

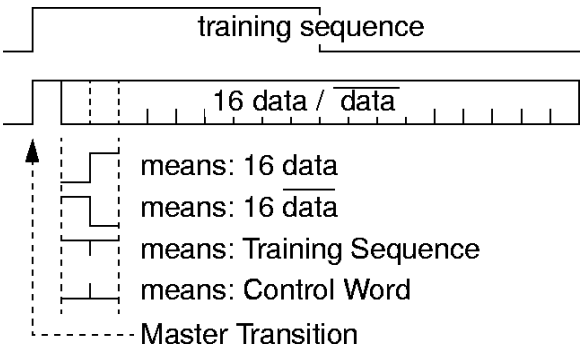

Fig. 3. Format of 16B/20B line code used with bang-bang CDR of.Fig. 2.

transition sample except for this master transition sample. During link start-up a training sequence is sent that has only one rising transition at the location of the master transition. Once the loop is locked, arbitrary data is allowed to be sent at the other 18 bits of the frame, while the transition sampler pays attention only to the data stream in the vicinity of the master transition. If the VCO frequency is too high, the transition flip-flop starts sampling prior to the master transition and outputs a "0" to the loop filter. A slightly lower VCO frequency, on the other hand, will cause the loop to be driven by 1's.

The loop drives the falling edge of the VCO into alignment with the data transitions based on the binary-quantized phase error. Because the clock-to-Q delay of the retiming flip-flop is monolithically matched with the phase detector flip-flop, the PLL aligns the recovered clock precisely in the middle of the data eye with no first-order timing skew over process and temperature variations. Because the narrowest pulse is the output of a flip-flop, such detectors operate at the full speed at which a process is capable of building a functioning flip-flop. This ensures that the phase detector will not be the limiting factor in building the fastest possible retiming circuit.

An additional advantage of flip-flop-based phase detectors is that since they only require simple processing of digital values, they easily generalize to multi-phase sampling structures allowing CDR operation at frequencies in which it would be impossible to build a working full-speed flip-flop. In contrast, most linear phase detectors require at least some analog processing at the full bit rate, limiting process speed and poorly generalizing to multi-phase sampling architectures.

Because of these compelling advantages, the bang-bang loop has become a common design choice for state-of-the CDR designs which are pushing the capability of available IC processes. Fig. 4 surveys CDR designs presented from 1988 to 2001 at the International Solid State Circuits Conference. Designs are plotted by year of presentation against each design's ratio of link speed to effective f_T. The majority of current designs utilize a combination of multiphase sampling structures and bang-bang PLLs. In addition, all CDRs operating at data rates greater than 0.4 f_T are bang-bang designs.

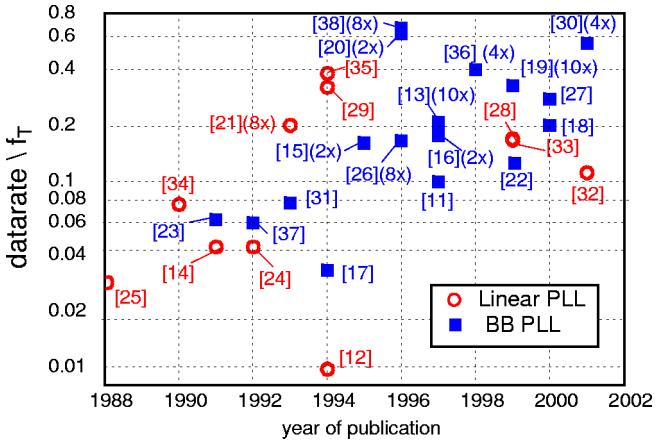

Fig. 4. CDR PLL designs over time. The ratio of link speed to effective process transit frequency is plotted vs year of publication. Multi-phase BB PLLs predominate as data rate approaches the process transit frequency limit. (The number of retiming phases used in each design is given in parentheses.)

II. First-order Loop Dynamics

Unfortunately, transition-sampling flip-flop-based phase detectors can provide only binary (early/late) or ternary (early/late + hold) phase information. This amounts to a hard non-linearity in the loop structure, leading to an oscillatory steady-state and rendering the circuit unanalyzable with standard linear PLL theory. Precise loop behavior can be simulated efficiently with time-step simulators, but this is cumbersome to use for routine design. Fortunately, simple approximate closed-form expressions can be derived for performance parameters of interest, such as loop jitter generation, recovered clock spectrum, and jitter tracking performance as a function of various design parameters.

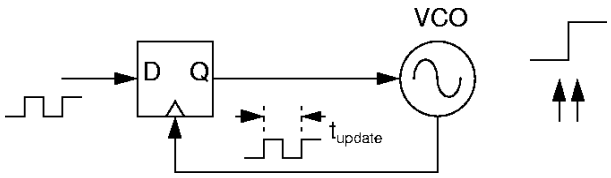

Fig. 5. A simple bang-bang loop using a flip-flop for a phase detector to lock onto square-wave input.

A simple BB PLL is shown in Fig. 5. A flip-flop is used as a phase detector to lock onto a square wave input signal. Depending on whether the VCO phase samples slightly before or after the rising edge of the input square wave, the flip-flop output is either low or high, adjusting the VCO period in such a way as to move the sampling phase error back towards zero. The dynamics of such a binary-quantized loop are equivalent to a data-driven phase detector operating on alternating 0,1 data with 100% transition density, or a master-transition based loop similar to that shown in Fig. 2. For simplicity, we assume that a valid binary phase determination can be made at every timestep. The consequence of random data

and the introduction of a ternary hold mode are considered in a later section.

The first-order BB PLL of Fig. 5 can be rendered into a block diagram for analysis as shown in Fig. 6. The loop phase error

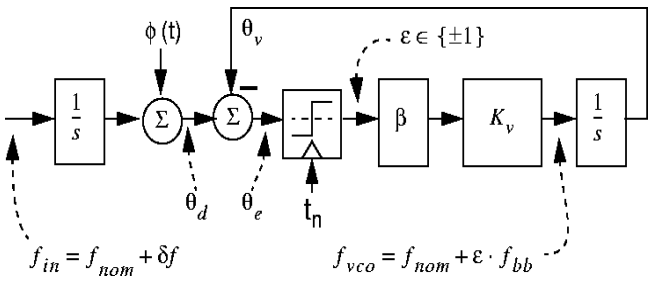

Fig. 6. Block diagram of first order loop showing definition of signal names.

$\theta_e(t_n)$, is defined as the difference between the data phase $\theta_d(t_n)$ and the VCO phase $\theta_v(t_n)$ at the nth sampling time t_n. For convenience, phase is measured with respect to an ideal clock source running at f_{nom}.

The frequency of the incoming data signal differs from the VCO center frequency by δf, and has a zero mean phase jitter of $\phi(t)$. In other words, the data can be considered to have been generated by a pattern generator clocked on the rising edges of the jittered clock signal $\sin[2\pi(f_{nom}+\delta f)t+\phi(t)]$. The data phase $\theta_d(t_n)$ is then $2\pi\delta f t_n + \phi(t_n)$.

The phase detector binary-quantizes the loop phase error at each sampling time to give $\varepsilon_n = \text{sign}[\theta_e(t_n)]$. (Note: In the case of a ternary data-driven phase detector, ε_n may be set to 0 when it is not possible to make a determination of phase error due to consecutive identical bits in the data stream. The consequence of this "hold" state is treated in a later section). The error signal drives the VCO through an attenuator β, to produce a change in frequency of $f_{bb} = \beta K_{vco}$. From time t_n until time t_{n+1}, the VCO operates at one of the two frequencies given by $f_{nom} + \varepsilon_n f_{bb}$.

Because the VCO frequency changes on each cycle, the system has non-uniform sampling times. The time of phase sample $t_{n+1} = t_n + 1/(f_{nom} + \varepsilon_n f_{bb})$. In a typical CDR, f_{bb} is on the order of 0.1% of f_{nom}, so that an analysis assuming uniform time steps of $t_{update} = 1/f_{nom}$ is sufficiently accurate for most purposes. However, for loop analyses requiring exact charge pump balance, such as wide-range loop pull-in without a frequency detector, these non-uniform sampling times must be accounted for.

With the uniform time step approximation, the VCO phase changes up or down (or "walks off") by $\theta_{bb} = 2\pi(f_{bb}/f_{nom})$ radians during each update period.

In summary, the first order loop obeys a simple set of discrete time difference equations:

$$\theta_d(t_n) = \theta_d(0) + 2\pi\delta f t_n + \phi(t_n) \quad (1)$$

$$\theta_v(t_{n+1}) = \theta_v(t_n) + \varepsilon_n\theta_{bb} \quad (2)$$

$$\varepsilon_n = \text{sign}[\theta_d(t_n) - \theta_v(t_n)] \quad (3)$$

As long as the VCO frequency step brackets the input signal frequency error, the loop will remain phase locked. Assuming $\phi(t)$ small, the lock range is: $-f_{bb} < \delta f < f_{bb}$. The loop generates an excess hunting jitter with a peak-to-peak value of two bang-bang phase steps $J_{pp} = 4\pi(f_{bb}/f_{nom})$.

For the loop to be locked, the average VCO frequency must equal the average data frequency. The phase detector duty cycle C, must satisfy the relation

$$\delta f = C(f_{bb}) + (1-C)(-f_{bb}).$$

The value of C is then given by

$$C = \left(\frac{1}{2} + \frac{\delta f}{2 f_{bb}}\right).$$

The phase detector duty cycle, and therefore its average output voltage are proportional to the loop frequency error. Fig. 7 shows a simulated loop with a range of input frequencies. The loop is

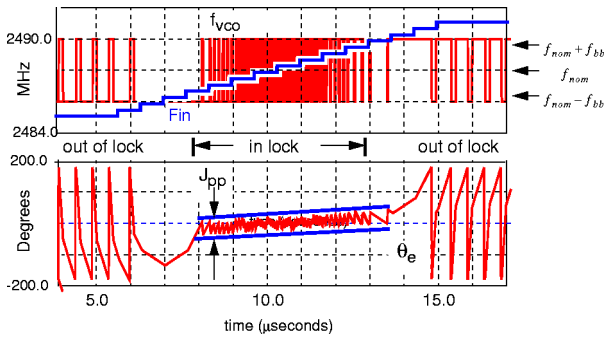

Fig. 7. Simulated response of first-order PLL to a range of input frequencies.

"locked" whenever the input frequency is bracketed by the two VCO frequencies. The rapid alternation between frequencies

slightly too high and slightly too low creates a bounded hunting jitter (J_{pp}).

The derivative of the input data phase deviation, $d[\phi(t)]/dt$, adds to the frequency error that must be tolerated by the loop. Assuming $\delta f = 0$, then for $\phi(t) = A\sin(2\pi f_{mod} t)$, the maximum amplitude A of phase modulation at frequency f_{mod} before onset of slew-rate limiting is $|f_{bb}|/f_{mod}$. Fig. 8. demonstrates the loop at the onset of jitter-induced slew-rate limiting. Although the average input frequency lies within the lock range of the loop, the added sinusoidal jitter causes the instantaneous input frequency deviation to exceed $\pm f_{bb}$. The loop stops toggling and goes into slew rate limiting, leading to a transient phase error.

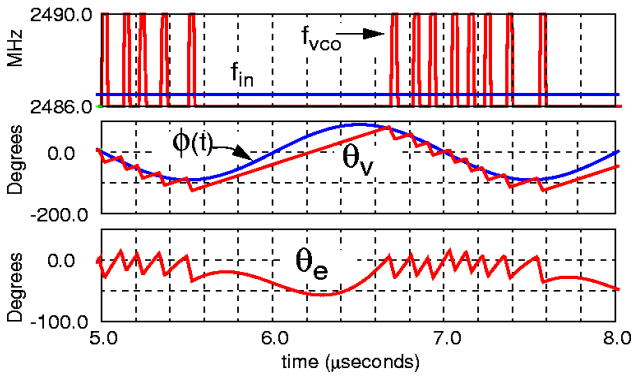

Fig. 8. Simulated response of first-order PLL to sinusoidal input jitter just slightly beyond the tracking capability of the loop.

A. Summary of First-Order Loop

The first-order bang-bang loop has only one degree of freedom. Jitter generation, lock range, and jitter tolerance are all inconveniently controlled by one parameter, f_{bb}. This situation can be improved by using a second control loop to dynamically adjust the nominal VCO frequency f_{nom} to be equal to the incoming data frequency. Because the phase detector duty cycle is proportional to the loop frequency error, this dynamic centering of VCO frequency can be accomplished by adjusting the VCO center frequency in a feedback loop to drive the phase detector duty cycle C to 50%. This decouples the lock range from jitter tolerance and jitter generation, giving more design freedom.

III. Second-Order Loop Dynamics

To extend the loop tracking range independent of the jitter generation, an extra integrator is added between the phase detector and the VCO as in Fig. 9. Since the first-order loop dynamic produces a phase detector duty cycle proportional to the loop frequency error, this added integrator can be viewed as an automatic means for keeping the first-order portion of the loop properly centered on the average incoming data frequency. If certain assumptions are met, as described later, we can consider the system to be composed of two non-interacting loops. These are the loops labeled "bang-bang branch" and "integral branch." If the center frequency control loop is slow enough, the resulting loop behavior will be very similar to a simple first-order loop, but with an extended frequency lock range.

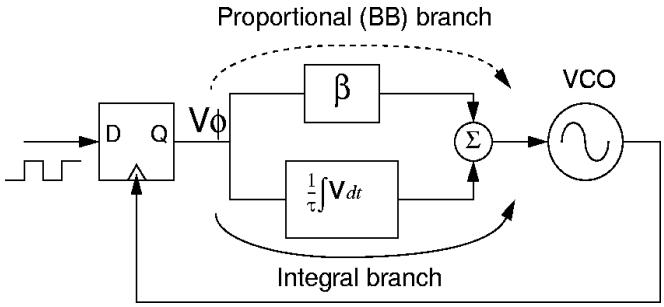

Fig. 9. Second-order bang-bang loop schematic.

A. Stability Factor

To preserve the desirable qualities of the first order loop, it is critical that the phase change due to the proportional branch dominate over the phase change from the integral branch.

The loop phase change in one update time due to the proportional connection is $\Delta\theta_{bb} = \beta V_\phi K_v t_{update}$. The phase change due to the integral branch is $\Delta\theta_{int} = V_\phi K_v t_{update}^2/(2\tau)$. The ratio of these two is the stability factor of the loop

$$\xi \equiv \frac{\Delta\theta_{proportional}}{\Delta\theta_{integral}} = \frac{2\beta\tau}{t_{update}}.$$

The reader should be careful not to confuse the bang-bang loop stability factor ξ with the linear loop damping factor ζ [5].

The discrete time difference equations for the second-order loop can be written as

$$\theta_d(t_n) = \theta_d(0) + 2\pi\delta f t_n + \phi(t_n) \quad (1)$$

$$\theta_v(t_{n+1}) = \theta_v(t_n) + \theta_{bb}\left(\varepsilon_n + \frac{\varepsilon_n}{\xi} + \frac{2}{\xi}\sum_0^n \varepsilon_n\right) \quad (4)$$

$$\varepsilon_n = \text{sign}[\theta_d(t_n) - \theta_v(t_n)] \quad (3)$$

From this, it can be seen that the second-order loop has two degrees of freedom, the loop phase step θ_{bb} (or equivalently, the loop frequency step f_{bb}) and the stability factor ξ. The added loop integrator extends the frequency tracking range, leaving θ_{bb} free to control jitter tolerance and jitter generation.

B. Simulations of Second-Order Loop

Fig. 10 shows two block diagrams for the second-order loop. The upper diagram is a straightforward translation of the schematic in Fig. 9. The lower diagram is a topological re-arrangement

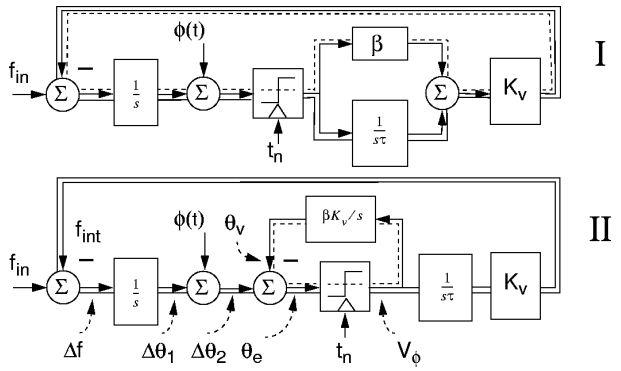

Fig. 10. Two equivalent second-order bang-bang loop block diagrams. The proportional phase-control signal flow is highlighted with a dashed line, and the integral frequency-control loop with a solid line.

which places an inner first-order phase tracking loop inside an outer frequency tracking loop. If one writes the transfer function from the output of the non-linear quantizer block back to the input of the quantizer, it can be shown that both diagrams are exactly equivalent. Some of the signals in the second diagram do not correspond to actual physical variables in the circuit, but they are helpful in understanding the operation of the loop.

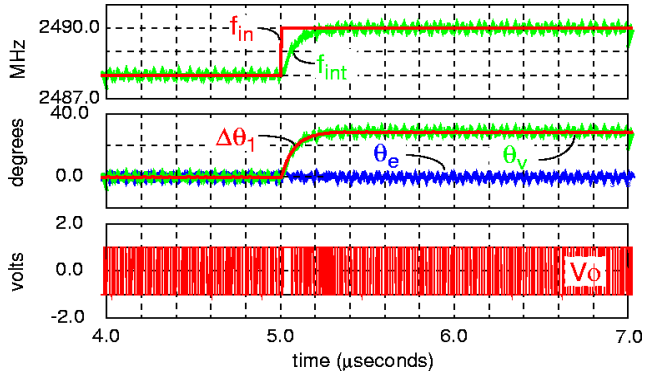

Fig. 11. Second-order loop response to instantaneous frequency step smaller than f_{bb}.

Fig. 11 shows the second-order loop responding to a step change in input frequency f_{in}, producing a slow response f_{int} in the outer integral loop. The resulting phase error $\Delta\theta_1$ is tracked by the inner bang-bang loop θ_v to produce the final sampler phase error θ_e. Notice that, unlike linear PLLs, if the power-supply noise-induced VCO frequency modulation is limited to $\pm f_{bb}$, then there is *no* jitter accumulation or phase transient at the sampling flip-flop.

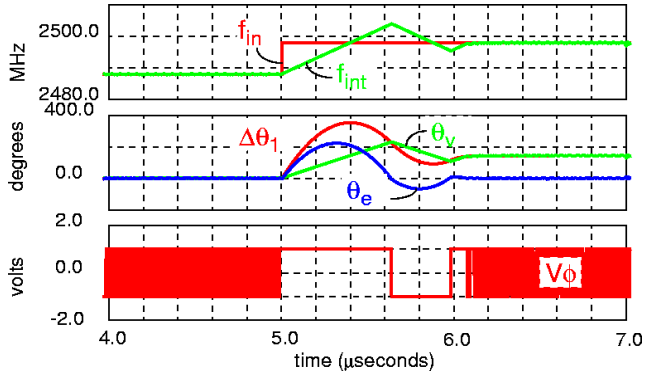

Fig. 12. Second-order loop response to instantaneous frequency step larger than f_{bb}.

Fig. 12 is a simulation in which the input frequency step is bigger than f_{bb}, so the loop goes into slew rate limiting, leading to a transient phase error θ_e at the sampler.

C. Response to Phase Step

For a normalized transient phase step of $\Delta = \theta_{step}/\theta_{bb}$, a first-order loop relocks in Δ update times. The total time for relocking is then $\theta_{step}/(2\pi f_{bb})$.

During the relocking transient of the second-order loop, the loop integrator overshoots the correct steady-state VCO tune voltage. This causes a quadratic overshoot in the phase trajectory.

Fig. 13 shows the second-order phase step response with ξ as a parameter. Up to the first zero crossing, the phase trajectory is given by

$$\frac{\theta(t)}{\theta_{bb}} = \Delta - \left(n + \frac{n^2}{\xi}\right),$$

with $n = t/t_{update}$. The time of the first zero crossing approaches Δ as $\xi \to \infty$, consistent with a first-order loop. In general, the second-order loop is quicker to reach zero phase error than the first-order loop, but pays for this with an oscillatory overshoot. As a conservative rule of thumb, the magnitude of the oscillatory transient of a second-order step response can be considered bounded by the simple linear transient of the first-order loop. The time required to reach steady state, given a step of Δ is always less than or equal to Δ timesteps, independent of ξ.

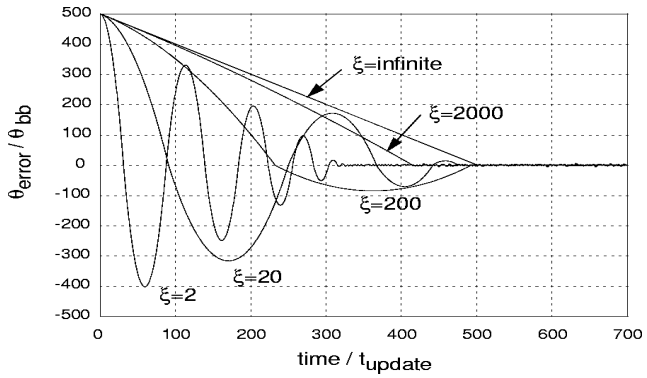

Fig. 13. Noise-free loop response to a phase step with stability factor ξ as a parameter.

IV. Slope Overload

Many systems, such as SONET, specify jitter tolerance in the form of a sinusoidal jitter at various frequencies.

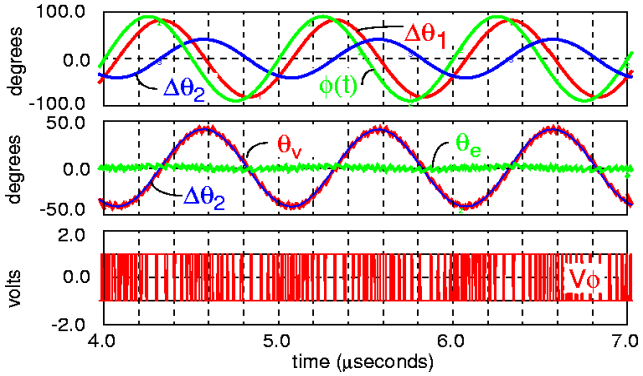

Fig. 14. Second-order loop response to sinusoidal input jitter.

Fig. 14 shows the loop response with a sinusoidal input phase jitter $\phi(t)$. The outer integral loop tracks the input jitter at $\Delta\theta_1$ with a slight phase lag. The resulting phase error $\Delta\theta_2$ is tracked by the inner bang-bang loop θ_v to produce the final sampler phase error θ_e. The duty-cycle of the PD output V_ϕ varies with the slope of $\Delta\theta_2$ which is proportional to the instantaneous frequency error of the outer loop.

In Fig. 15, the phase modulation is increased until the instantaneous frequency error exceeds the inner loop's ability to track. Slew-rate limiting produces a tracking error at the sampler θ_e. A CDR would normally be designed such that slewing would never occur for any valid signal allowed by a particular standard. The next two sections develop an analytic expression for slope overload so that a loop can be easily designed to never slew for signals meeting a typical frequency-domain jitter tolerance specification.

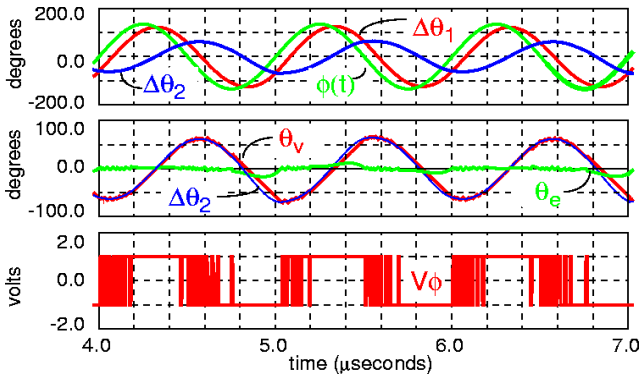

Fig. 15. Second-order loop response to large sinusoidal input jitter.

A. Delta-Sigma Analogy

Before developing an analytic equation for slope overload, it is helpful to introduce a further rearrangement of block diagram II from Fig. 10. Fig. 16 transforms the loop by pulling two integrators through the last summing node prior to the quantizer. The update time interval is set to 1. The definition for bang-bang frequency step $f_{bb} = \beta K_v V_\phi$, and stability factor $\xi = 2\beta\tau/t_{update}$ are also substituted in.

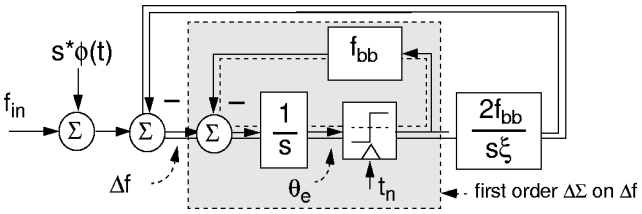

Fig. 16. Redrawing of the loop to show inner $\Delta\Sigma$ inner modulator operating on the loop frequency error.

The shaded area in Fig. 16 shows how the proportional feedback loop can be thought of as an inner $\Delta\Sigma$ modulator producing a phase detector duty cycle proportional to the VCO frequency error [6],[7].

Fig. 17 summarizes an analysis of the first order delta-sigma (after [8]). When the loop is not in slew rate limiting, or in a periodic limit-cycle, the quantizer (e.g., PD) can be replaced with a unity gain element and a noise source $Q(z)$ with the same $A\sin(2\pi tft/t_{update})/(2\pi ft/t_{update})$ noise characteristics as a random binary bitstream. Both these constraints are met in practice as the VCO phase noise is sufficient to eliminate any deterministic limit cycles, and the loop is designed to never slew rate limit on any conforming input signal. This insight is critical as

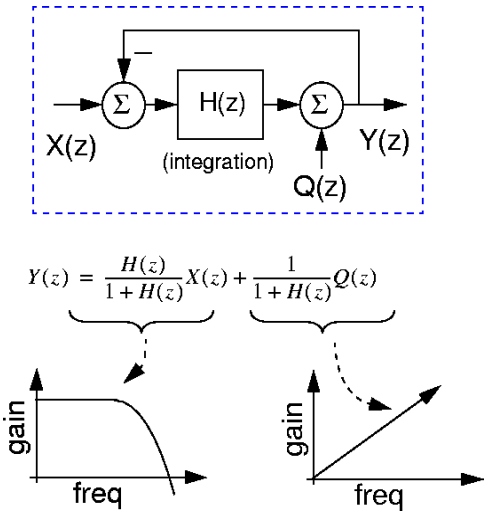

Fig. 17. Simplified analysis of delta-sigma circuit.

it allows linear analysis to be applied whenever the bang-bang loop is not in slew rate limiting.

With the $\Delta\Sigma$ substitution, the inner loop becomes a wide-band unity-gain block as seen from the viewpoint of the outer integral frequency control loop. The noise in the delta-sigma core is first-order frequency shaped towards high frequencies. However, when the frequency noise is converted to phase noise, the shaping is lost and the noise becomes flat.

B. Expression for Slope Overload

A closed-form analysis of slope overload can now be derived. Referring to Fig. 16, the system slews when $|\Delta F| > f_{bb}$. Assuming no slew rate limiting, we can use the results from the $\Delta\Sigma$ analysis to justify replacing the loop quantizer with a unity gain element. The maximum input phase jitter in UI as a function of frequency, $\sigma_j^{max}(s)$, normalized to θ_{bb} can then be calculated using Laplace transforms.

We want to find an input excitation $F(s)$, for which $|\Delta F| = f_{bb}$ at all frequencies. The inner $\Delta\Sigma$ of Fig. 16 has a linearized transfer function of $1/(s + f_{bb})$. Using standard feedback loop theory, the expression for ΔF can then be written as

$$\Delta F = \frac{F(s)}{1 + \left(\frac{2 f_{bb}}{s\xi}\right)\left(\frac{1}{s + f_{bb}}\right)}.$$

Setting $\Delta F = f_{bb}$, and normalizing the equation by letting f_{bb} and $t_{update} = 1$, we can solve for $F(s)/s$ to get the maximum normalized input phase as a function of normalized frequency

$$\frac{\sigma_j^{max}(s)}{\theta_{bb}} = \left(\left(s^2 + s + \frac{2}{\xi}\right)/(s^3 + s^2)\right).$$

This is a curious bootstrapped analysis, in that it assumes a lack of slewing to justify the linearization which permits the computation of the onset of slew rate limiting.

Fig. 18 shows a good agreement between this expression and simulated loop performance in which slewing is defined as a contiguous sequence of ten or more identical phase-error indications. This expression can be used to design a loop for a given jitter tolerance. The tolerance plots are single-pole slope for high ξ and high jitter frequency, becoming double-pole at lower frequencies and small ξ. At high frequencies, all of the curves become asymptotic to the single-pole tolerance of a first-order bang-bang PLL. The operating region below each of these curves is where the $\Delta\Sigma$ approximation is valid, and where a linear loop analysis is justified.

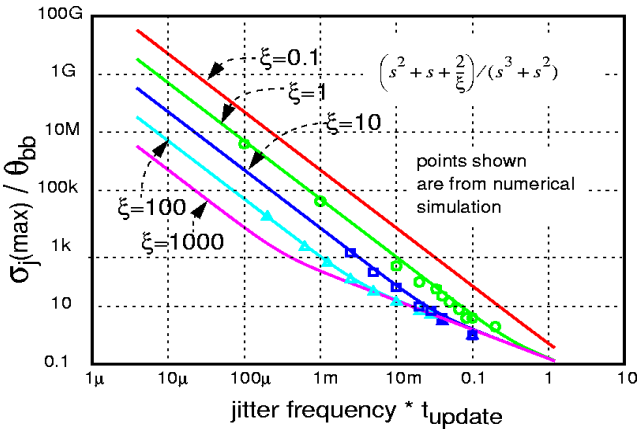

Fig. 18. Normalized amplitude of sinusoidal jitter just sufficient to cause slope overload as a function of normalized jitter frequency and with ξ as a parameter.

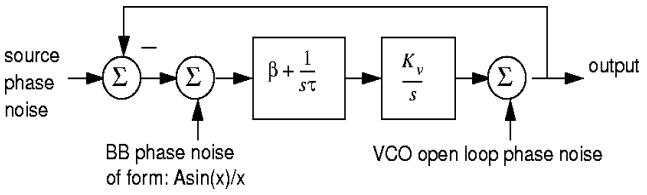

Fig. 19. Loop redrawn replacing phase detector with unity gain element and additive quantization noise.

V. Jitter Generation

With these insights, it is possible to accurately predict the loop jitter generation in the frequency domain. Fig. 19 is a redrawing of the loop replacing the phase detector by a unity gain element, and an additive noise source. The forward loop gain is

$$H(s) = \frac{K_{vco}}{s}\left(\beta + \frac{1}{s\tau}\right).$$

From this can be calculated two transfer functions: the lowpass seen by both the source phase noise and the PD noise to the output, $A(s) = 1/[1 + H(s)]$, and the high-pass transfer function from VCO phase noise to the output, $B(s) = H(s)/[1 + H(s)]$. As shown in Fig. 20, with a source phase noise P(s), a PD phase noise Q(s), and a VCO phase noise R(s), the total loop jitter generation spectrum becomes the RMS combination of each of the three weighted terms $J(s) = \sqrt{(PA)^2 + (QA)^2 + (RB)^2}$. The source phase noise is

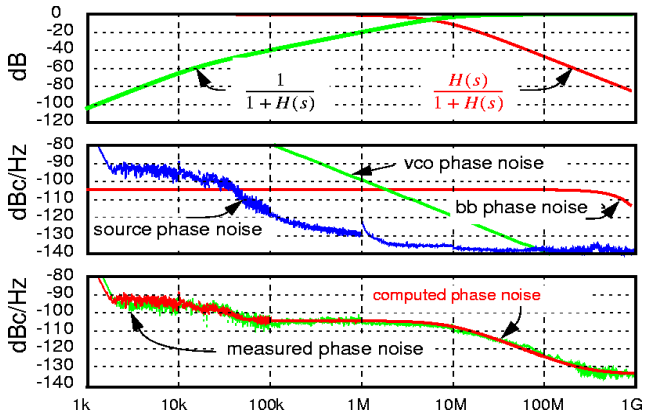

Fig. 20. Example computation of loop jitter generation spectrum with parameters from [11].

generally taken to be the spectrum of the clock driving the data source or BERT, or in the case of a clock multiplying circuit, the spectrum of the reference clock corrected by 20 times the log of the loop frequency multiplication ratio.

The phase noise power is given by

$$S_{RMS} = \int_0^{w_{max}} J^2(s)d\omega.$$

The RMS jitter in unit intervals is then $J_{RMS} = \text{atan}(\sqrt{S_{RMS}})/\pi$.

It should be noted that the linearized loop model is only suitable for computation of the jitter spectrum but not for computing the actual sampling point phase error or other time-domain transient response. The linearized response only covers the dynamics of the outer frequency tracking loop, but does not capture the extra tracking of the internal nonlinear $\Delta\Sigma$ core.

VI. Gaussian Input Noise

Fig. 21 is a plot of output jitter vs input jitter with ξ as a

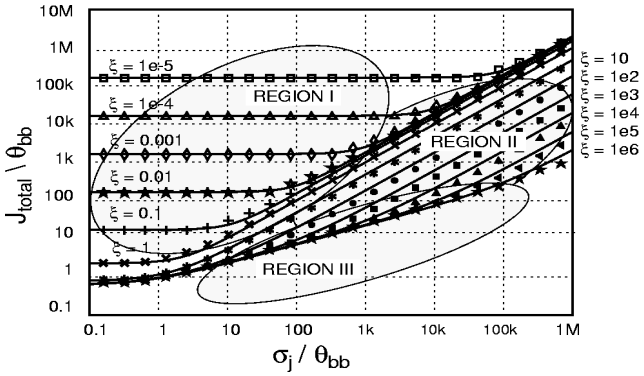

Fig. 21. Normalized output jitter vs input jitter sigma with ξ as a parameter. Simulation is for a non-tristated loop, with square wave data input, 10^8 timesteps per point, and ignoring phase wrapping.

parameter. For convenience, all jitter sigmas are normalized to θ_{bb}, the loop phase step size. The total loop output jitter can be approximated by three regions of operation: $J_{total} \approx J_{idle} + J_{linear} + J_{walk}$. In Region I, the output jitter is independent of input jitter σ_j. This occurs when the self-generated hunting jitter exceeds the input jitter. The RMS jitter in this region is empirically determined to be well approximated by $J_{idle} \approx 0.6 + (1.65/\xi)$. In Region II, the output jitter is proportional to the input jitter. This occurs when the input jitter is so high that, for a given ξ, the bang-bang dynamic is unable to control the second-order portion of the loop. This leads to large quadratic trajectories in the phase domain, causing the loop phase to "hunt" towards the limits of the input jitter distribution. As the loop phase nears the limits of the input jitter distribution, the bang-bang hunting has more effect on stabilizing the second-order loop. In this region, the output jitter is proportional to the input jitter: $J_{lin} \approx 2\sigma_j/(1 + \sqrt{\xi})$. In Region III, the output RMS jitter J_{walk} is approximately equal to $0.7 \cdot \sqrt{\sigma_j}$. This surprising result says that loops with large ξ have output jitter which grows as the square root of the input jitter. Contrast this with a linear PLL which simply low-pass filters the input jitter and thus has an output jitter which grows linearly with the input jitter.

An approximate analysis of loop jitter can shed light on this curious square-root dependence of output jitter on input jitter. Assume a zero-mean input jitter distribution with a sigma σ_j. Using a linearized approximation to the standard probability distribution function, the probability of getting an "early" phase error indication for small loop phase deviation $\Delta\theta$, is approximately

$$p_e \approx \frac{1}{2} - \frac{\Delta\theta}{\sigma_j\sqrt{2\pi}}.$$

The expected phase change in the loop after one update time is

$$\theta_{bb}((1-p_e)-p_e) = \frac{2\Delta\theta}{\sigma_j\sqrt{2\pi}}\theta_{bb}$$

The discrete time equation for the average evolution of loop phase under the condition of a small input phase error can then be expressed as

$$\Delta\theta(t_{n+1}) = \left(1 - \frac{2\theta_{bb}}{\sigma_j\sqrt{2\pi}}\right)\Delta\theta(t_n),$$

This equation has the same form as a discrete time approximation to the capacitor voltage in an RC lowpass filter. By analogy, when time is expressed in units of loop update times, any transient phase error in the bang-bang loop can then be said to decay to zero with a time constant of $\tau = \sigma_j\sqrt{2\pi}/(2\theta_{bb})$.

This "lowpass" loop characteristic is being driven by random energy from the early/late phase detector output. A related problem is the computation of the baseline wander voltage generated by passing a random NRZ data stream through a coupling capacitor. It can be shown that the sigma on the capacitor voltage is given by $\sigma_{BLW} = V_{pp}\sqrt{t_{bit}/(8\tau)}$. Extending this analogy to the loop, we can consider the output of the phase detector as a 50% duty-cycle random NRZ data stream. Given that the output from each "bit" must cause a loop phase change of θ_{bb} , we can compute that the effective V_{pp} to satisfy our loop difference equation must be $\sqrt{2\pi}\sigma_j$. We can then compute the loop jitter by using the analogous baseline wander expression with the effective loop V_{pp} and τ . The result is

$$\sigma_{bb} = \sqrt{\frac{\theta_{bb}\sigma_j\sqrt{2\pi}}{8}} \approx 0.79\sqrt{\theta_{bb}\sigma_j},$$

which is consistent with empirical analysis of simulation results.

One further insight into this behavior is offered. The second-order loop drives the phase detector output to a steady-state 50% duty-cycle. In this condition, the loop phase splits the input jitter distribution into equal early and late halves. This means that the bang-bang loop phase is servoed to the *median* of the input jitter distribution rather than to the *mean* as would be the case with a linear loop. Because of this, the bang-bang loop makes a constant modest correction in response to large jitter outliers, rather than the proportionally large overcompensation of a linear loop. This insight supports the idea that the bang-bang loop jitter should only be sub-linearly affected by the magnitude of the input jitter.

VII. Data-Driven Phase Detectors

Unless the data contains a guaranteed periodic transition, the CDR will be required to lock onto random transitions embedded in the data stream. The effects of runlength and transition density on loop performance must then be considered. The effect of these two data attributes is dependent on the type of phase detector used. Most modern codes use some variation of Alexander's phase detector [9] shown in Fig. 22.Two matched flip-flops form the front-end of Alexander's phase detector, with the first flip-flop driven on the rising edge of the 50% duty-cycle clock, and the second flip-flop driven on the falling edge of the same clock. (Using a fully-differential monolithic ring-oscillator, it is possible to achieve a very precise 50% duty-cycle clock source). When the loop is locked, the rising-edge retiming flip-flop samples the center of each data bit and produces a retimed data bit at (A) and the following retimed bit at (B). The falling-edge flip-flop functions as a phase detector by sampling the transition (T) between the data bits (A,B). To improve the circuit's operating speed, the (T) sample is delayed an extra half bit time by a latch so that the logic on (A,T,B) has a full bit time for resolution.

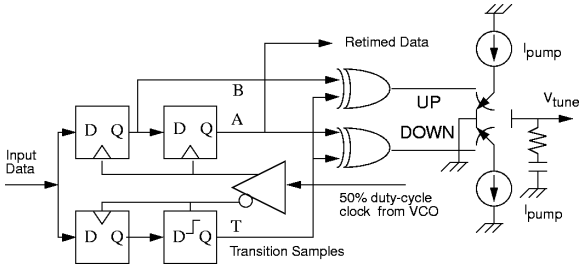

Fig. 22. Modified form of Alexander's ternary-quantized phase detector for NRZ data along with a typical charge pump for driving the VCO tuning input.

The transition sample is then compared to the surrounding data bits to determine whether the clock sampling phase is early or late to derive a binary-quantized (bang-bang) or ternary phase error indication. A truth-table for the logic in Fig. 22 is given in Table 1.

TABLE 1. Truth table for logic in Fig. 22.

State	A	T	B	UP	DOWN	Meaning
0	0	0	0	0	0	hold
1	0	0	1	0	1	early
2	0	1	0	1	1	hold
3	0	1	1	1	0	late
4	1	0	0	1	0	late
5	1	0	1	1	1	hold
6	1	1	0	0	1	early
7	1	1	1	0	0	hold

The states 2 and 5 in Table 1 correspond to the normally impossible condition of sampling a "1" midway between two "0" bits. A custom truth table can use these states to detect either a high bit-error-rate condition [10], a VCO running grossly too slowly (eg: lump these states into the "late" condition), or taken as an indication that a link has locked onto its own VCO crosstalk, perhaps by amplification of power supply noise by pick up from a high-gain optical transimpedance amplifier [11].

Since the mid-bit samples (A,B) straddle the (T) transition sample, it is also possible to detect the lack of a transition. This condition corresponds to states 0 and 7 in Table 1. This information can be used to create an extra ternary hold-state in the PD output, causing the charge pump to hold its value during long runlengths. Both binary and ternary PDs will be discussed in turn, along with their implications on loop performance.

A. Run-length and Latency

Binary phase detectors have no hold state, so the PD continues to put out the last valid phase error indication during long data runlengths. In this situation, the loop idling jitter will be multiplied from the expected value by the maximum runlength of the data. For example, an 8B/10B code has a maximum code runlength of 5 and will have a peak jitter walk-off five times the value of that computed for a "10" repetitive data pattern. The average RMS jitter will be a function of the runlength distributions of each particular code. There is also a trade-off in effective stability factor as a repetitive pattern such as "11110000" will be equivalent to a loop with an effective update time 4 times larger than the expected $t_{update} = 1/f_{nom}$. Since the stability factor is inversely dependent on update time, it is possible for binary PDs to become unstable with data patterns containing very long runs due to the delay in timely phase-error feedback.

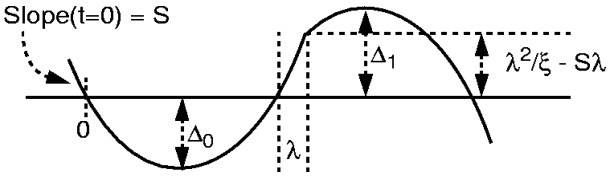

Fig. 23. Setup for computing onset of loop instability with latency λ.

Fig. 23 shows the loop phase trajectory during an acquisition transient. At t=0, the loop crosses zero phase error with $d\phi/dt = S$. From this we can compute an overshoot Δ_o. When the loop phase again crosses zero phase error, the phase detector is late in responding by a time λ. This time is a combination of runlength, latency in the phase detector logic, and high-order poles in the VCO tuning characteristic.

Due to the loop latency λ, the loop overshoots zero phase by $\lambda^2/\xi - S\lambda$ before the "braking" effect of the proportional branch starts to act. The onset of catastrophic instability occurs when $\Delta_1 > \Delta_0$, for this implies exponential growth of the acquisition transient. The convergence is guaranteed whenever $\xi > 2\lambda$.

Although usable for tightly constrained block codes such as 8b/10B, binary phase detectors are essentially unusable for codes such as 10Gb Ethernet 64b/66b or SONET which can have very long runlengths of up to 66 or 80 bits, respectively.

B. Ternary Phase-Detector

The 3-state, or ternary phase detector provides superior jitter performance for data with long runs [12]. Ternary PDs neither charge nor discharge the loop filter during long runs causing the loop to hold the current estimate of the data frequency. Such loops effectively "stop time" during long runs.

If the charge pump does not have a hold-mode, it is possible to emulate a ternary loop, with some loss of performance, by continuously toggling the phase-detector output to approximately maintain the current charge pump voltage during long runs.

The peak idling jitter for ternary loops is unchanged from the simple 100% transition density analysis. The RMS jitter will be reduced by the average transition density. Because the loop phase cannot change during hold mode, the jitter tolerance will be derated by the average transition density. This can easily be taken into account by increasing θ_{bb} appropriately for the characteristics of the code to be used.

C. VCO Tuning Bandwidth

The previous analyses all assumed an infinite VCO tuning bandwidth for the proportional tuning input. A VCO time-constant τ_{vco}, can slightly reduce hunting jitter if it is small compared to the loop update time.

Timeconstants larger than the loop update time prevent the loop from reversing phase slope within an update period and lengthen the loop limit cycle. If the extra pole is thought of as an extra latency $2\tau_{vco}$, then the result of the previous section can be used to give an approximate bound on loop stability. To avoid divergence: $\tau_{vco} < \xi t_{update}/4$. Comparison with simulation verifies this equation as a conservative limit on τ_{vco}.

However, it cannot be recommended to flirt with this boundary. Unless one meticulously checks performance by numerical simulation, it is safest to design the VCO to essentially respond fully in one update time. This is usually very easy to achieve in ring-oscillators and possible with some care using low-Q LC VCOs.

VIII. Conclusion

Bang-bang CDR circuits have the unique advantages of inherent sampling phase alignment, adaptability to multi-phase sam-

pling structures, and operation at the highest speed at which a process can make a working flip-flop. Approximate equations for loop jitter, recovered clock spectrum, and jitter tracking performance as a function of various design parameters have been derived. The median-tracking property of the bang-bang loop resulting in an output jitter equal to the square root of the input jitter has been presented.

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Richard Walker was born in San Rafael CA, in 1960. He received the B.S. degree in Engineering and Applied Science from the California Institute of Technology in 1982, and an M.S. degree in Computer Science from California State University, Chico, CA in 1992. Rick joined Agilent Laboratories (formerly Hewlett-Packard Laboratories) in 1981, where he is currently a Principal Project Engineer. Since that time, he has worked in the areas of broadband-cable modem design, solid-state laser characterization, phase-locked-loop theory, linecode design, and gigabit-rate serial data transmission. He holds 15 U.S. patents.