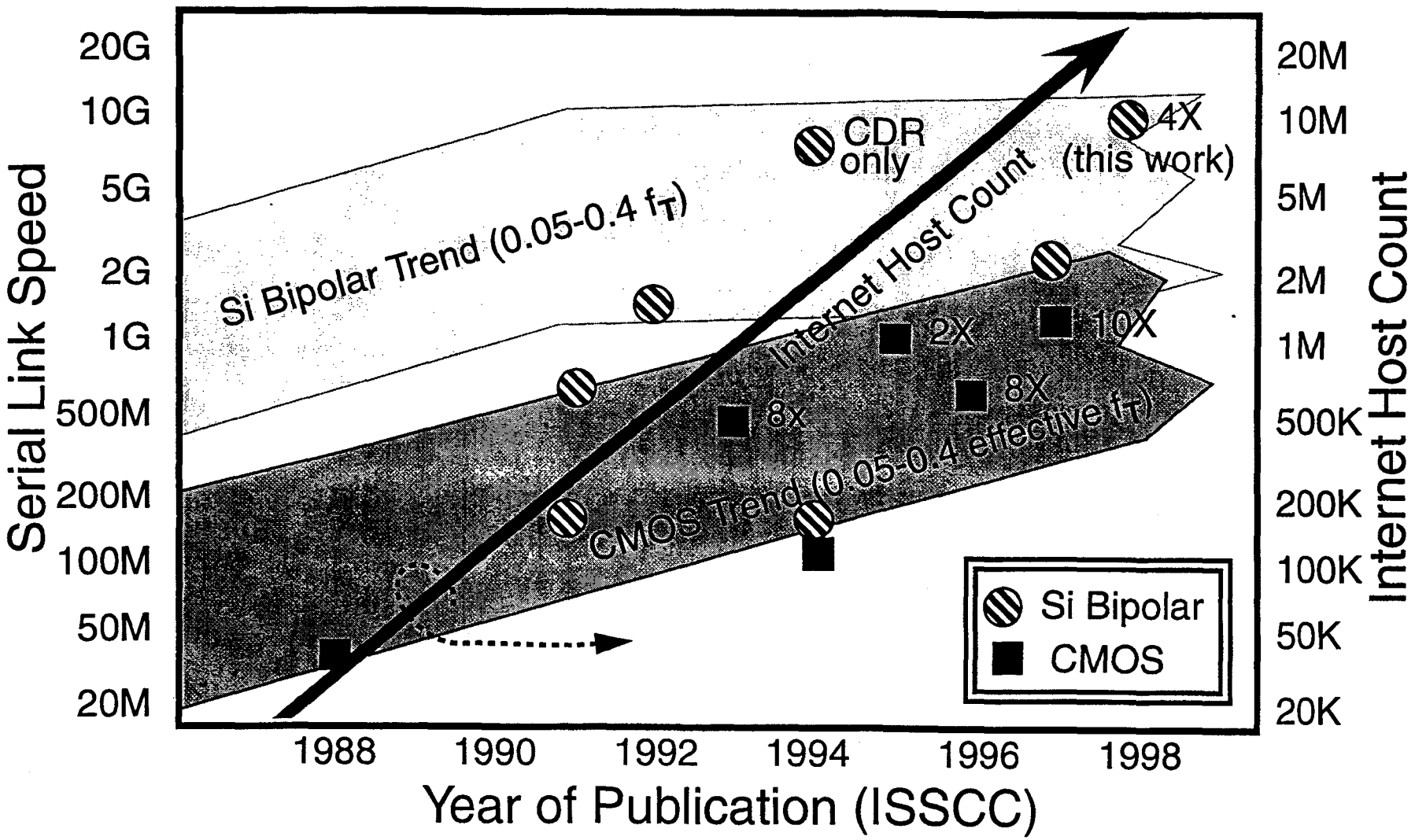
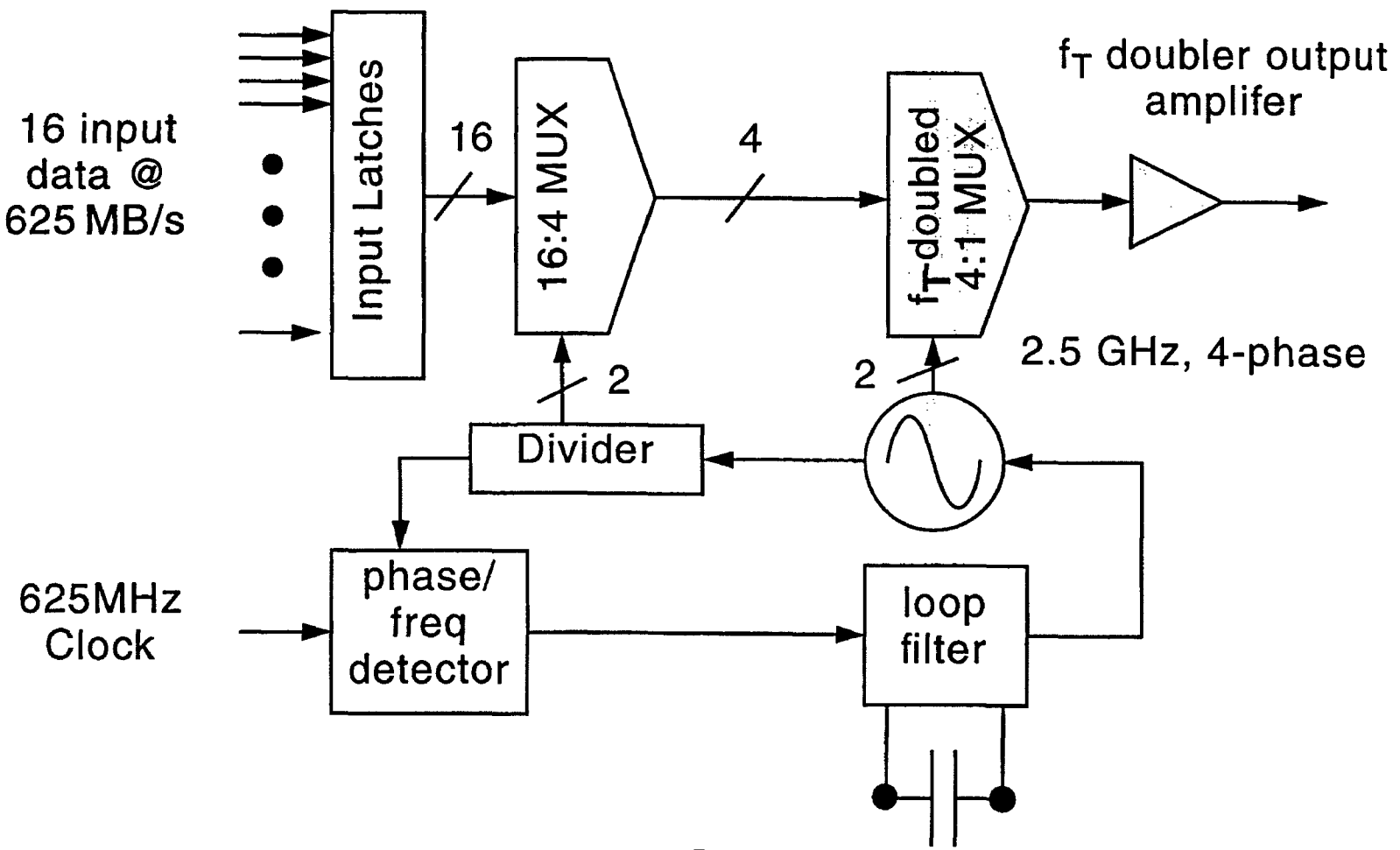
Outline

- Motivation
- TX/RX Block Diagrams
- Multi-phase VCO
- f_T-doubler Designs (Amp, Mux)
- Measured Performance
- Package
- Die Photos and Summary

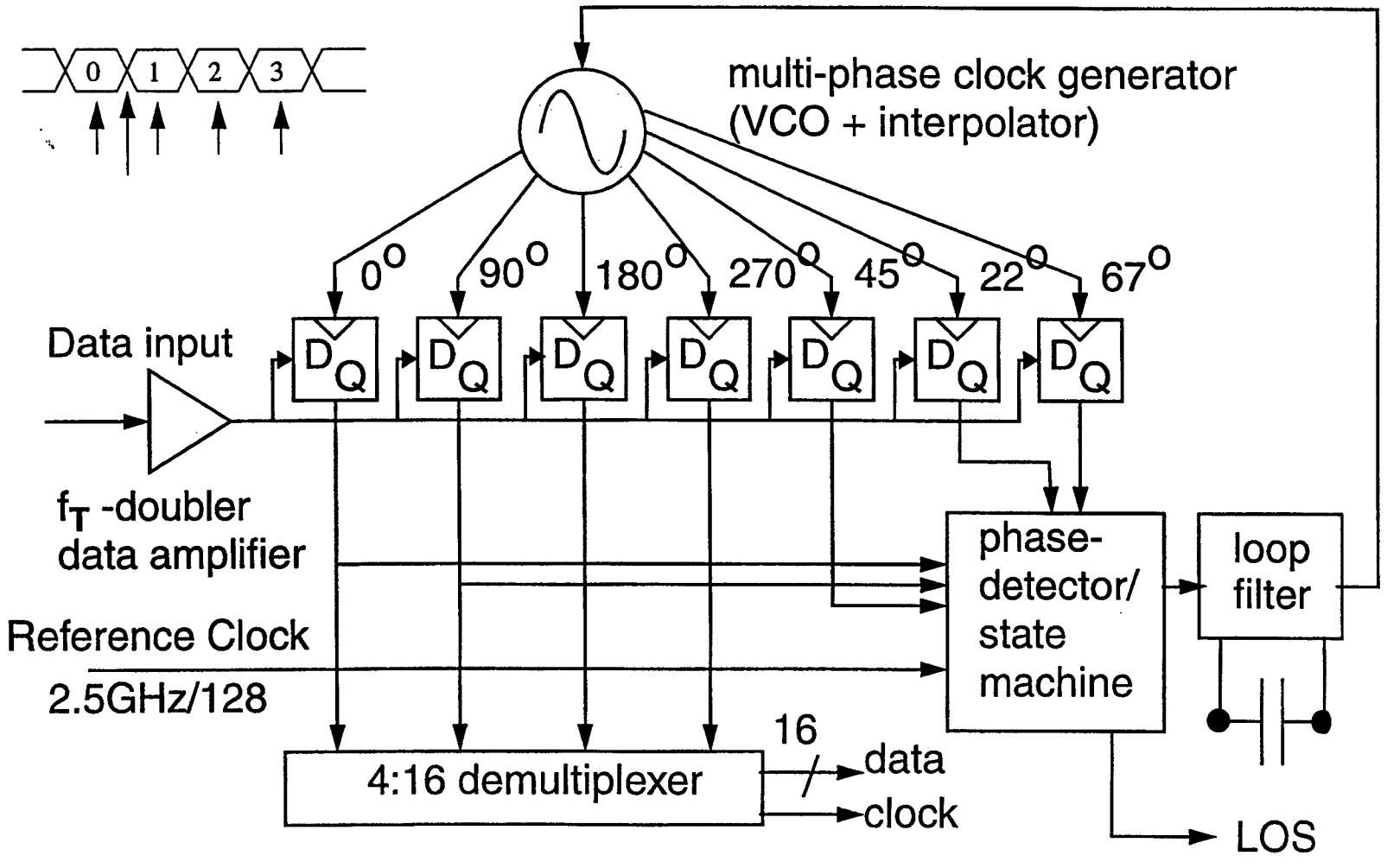
Communication Trends



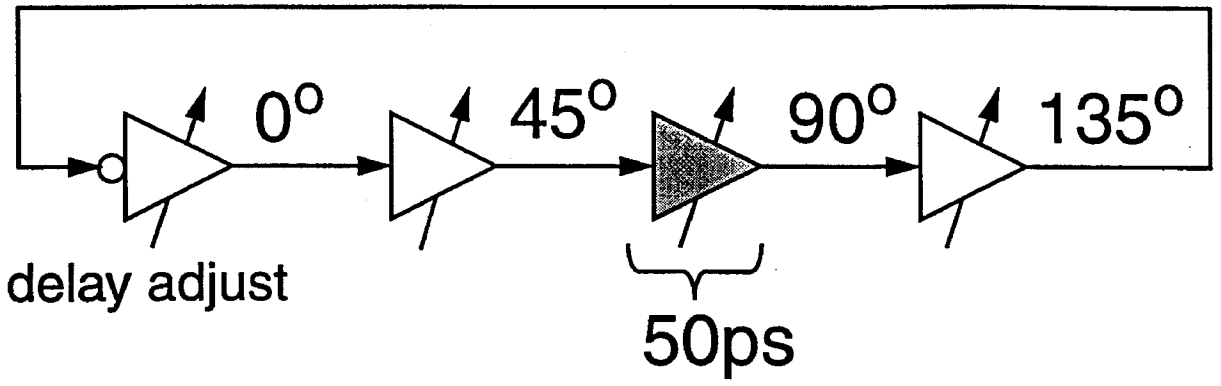
Transmitter Block Diagram

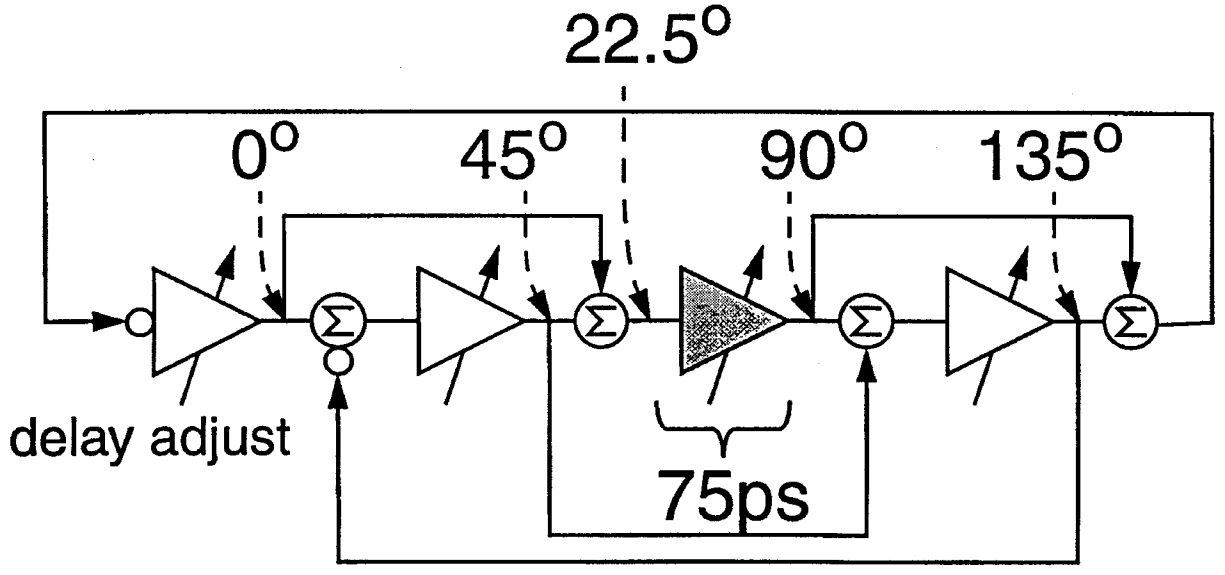


Receiver Block Diagram

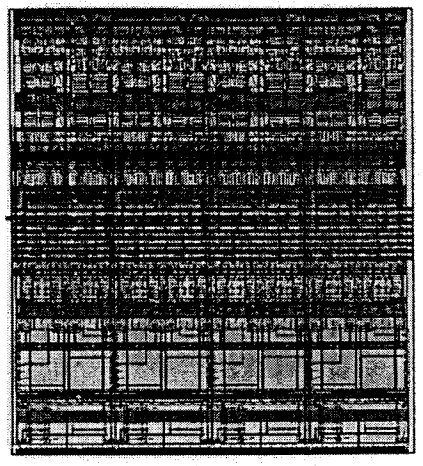


VCO Block Diagram



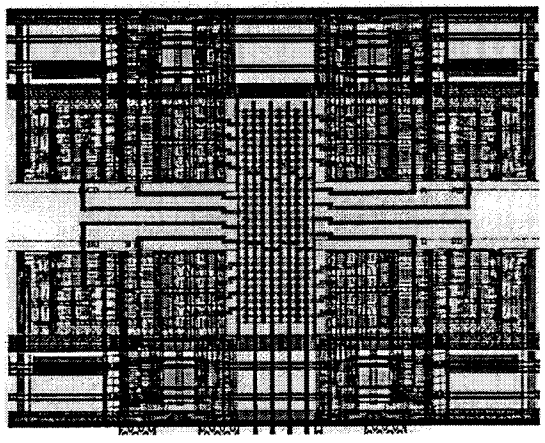


VCO Layout Issues



Simple linear layout

- achieves 7ps peak error between phases (simulated)
- limited by interconnect resistance mismatch



Quad symmetric layout

- achieves 1ps peak error (simulated)
- interconnect resistances and capacitances are matched

f_T-doubler Advantages

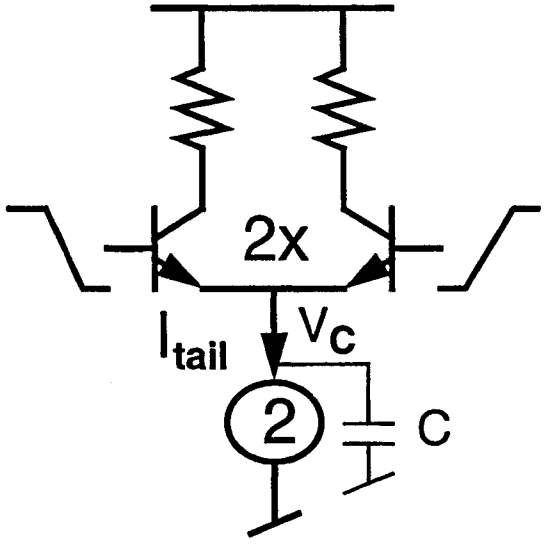
Provides lower input capacitance

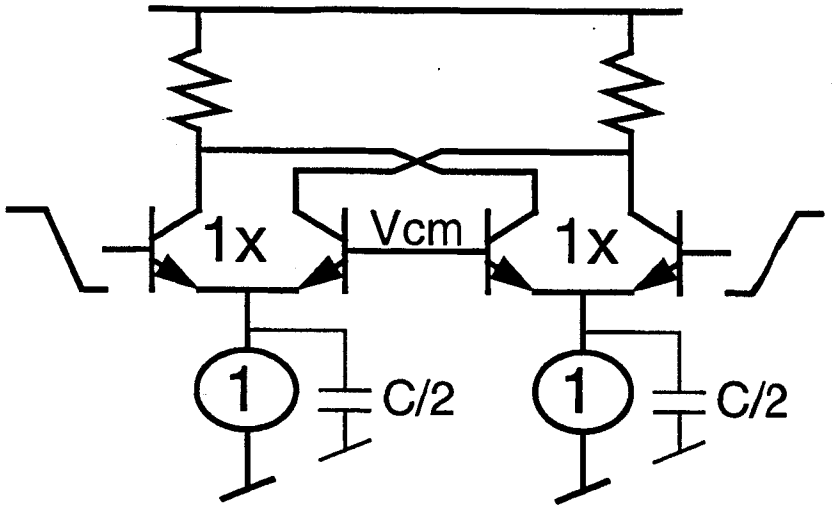
- less loading on previous stage

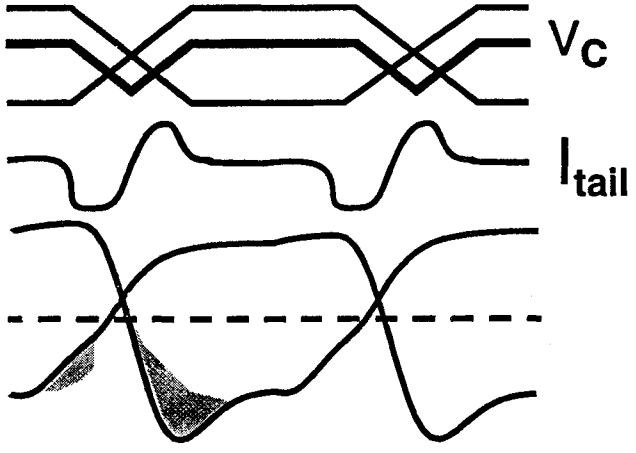
Provides better output waveform symmetry

- less pattern dependence and jitter

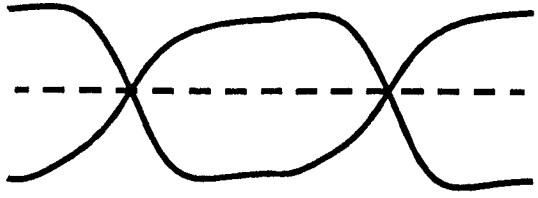
Diff-pair versus f_T-doubler



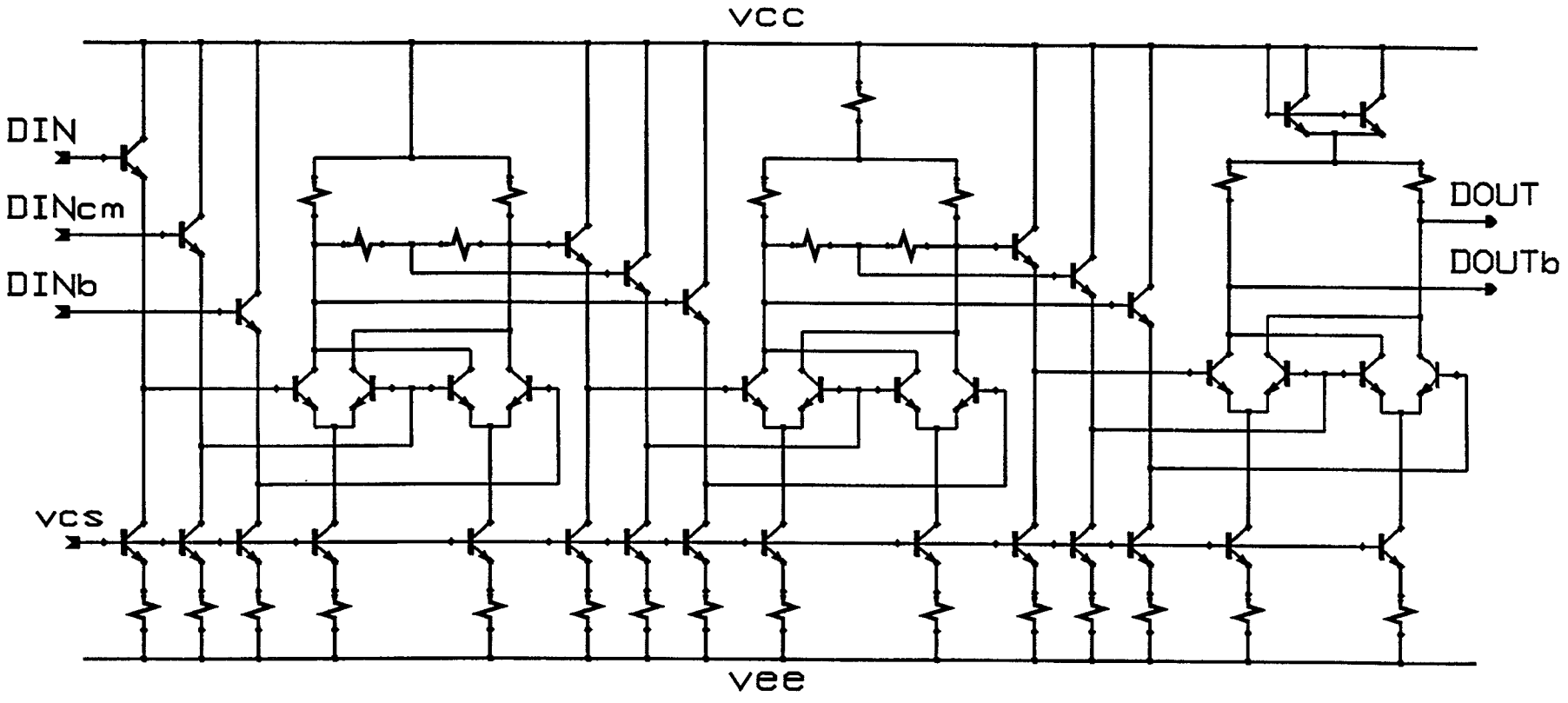




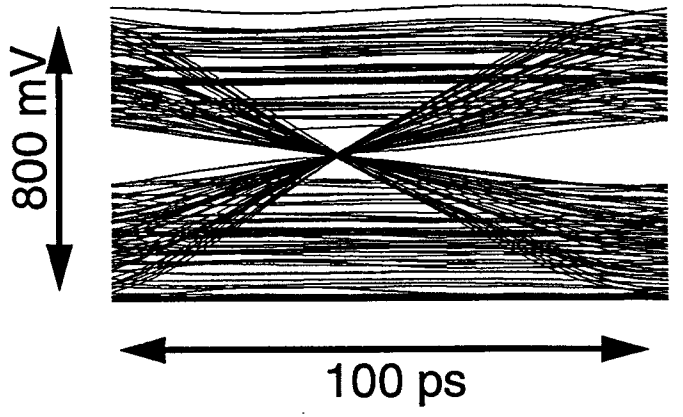
Parasitic current source and device capacitance is 1/2 diff-pair value giving a more symmetric output

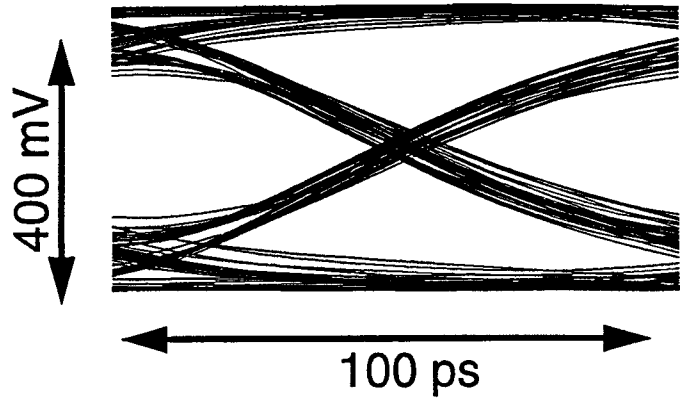


3-Stage f_T-doubler Amplifier



3-Stage f_T-doubler Amplifier (simulated)





Input torture test:

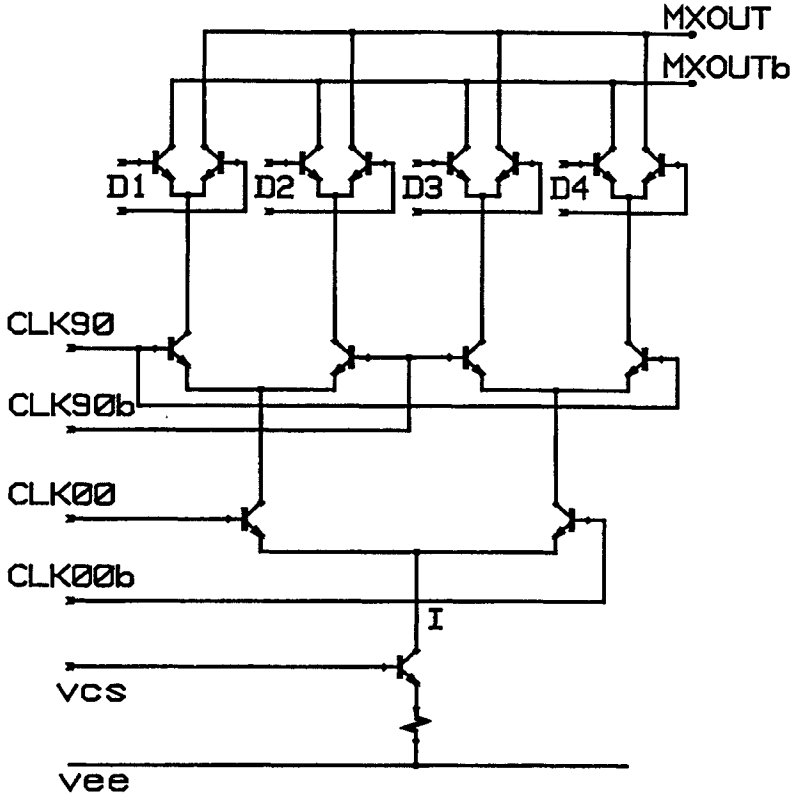
- 2^7-1 PRBS signal with randomly varying pulse amplitudes, stresses both AM and phase margins

Output of amplifer:

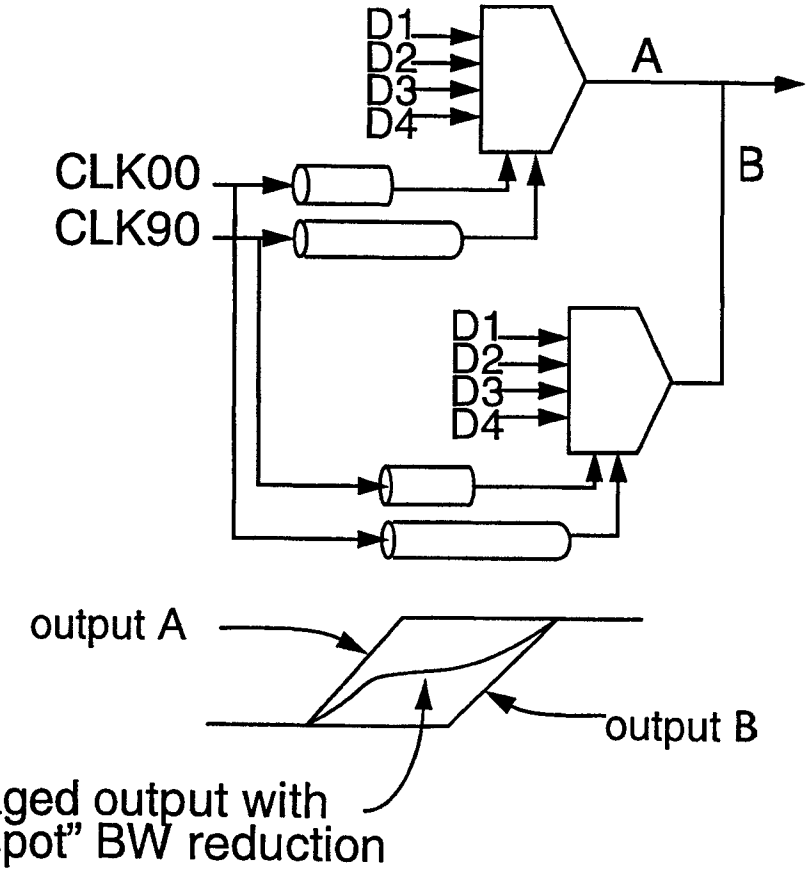
- Driving 8 latches at 10Gb/s
- Simulation includes package, bond wires and ESD protection
- 3 ps jitter due to package
- 10ps (p-p) from amplifier

Traditional non-retimed 4:1 Multiplexer

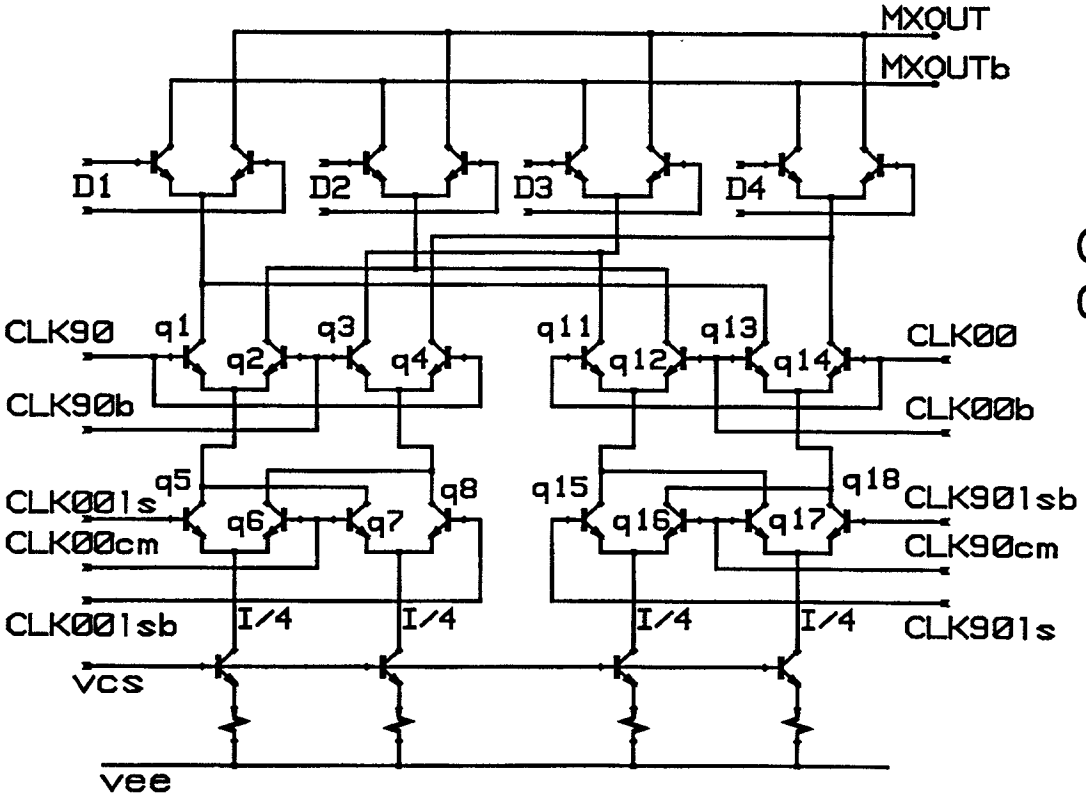
Simple 4:1 Mux

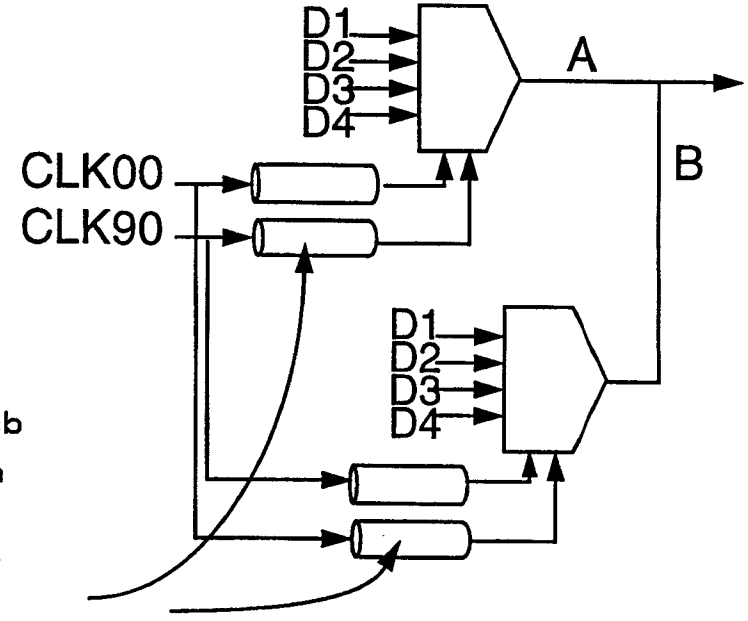


Using Two Muxes for Symmetry



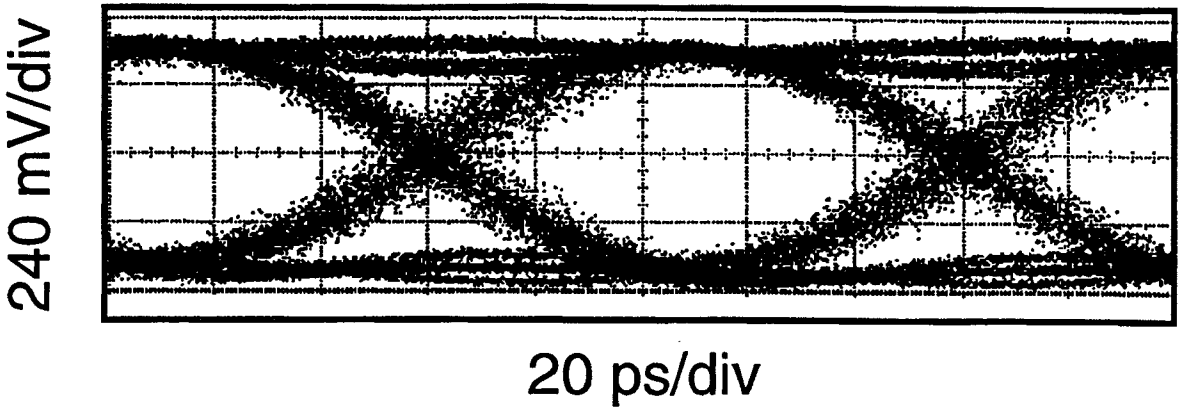
f_T-doubler 4:1 Multiplexer





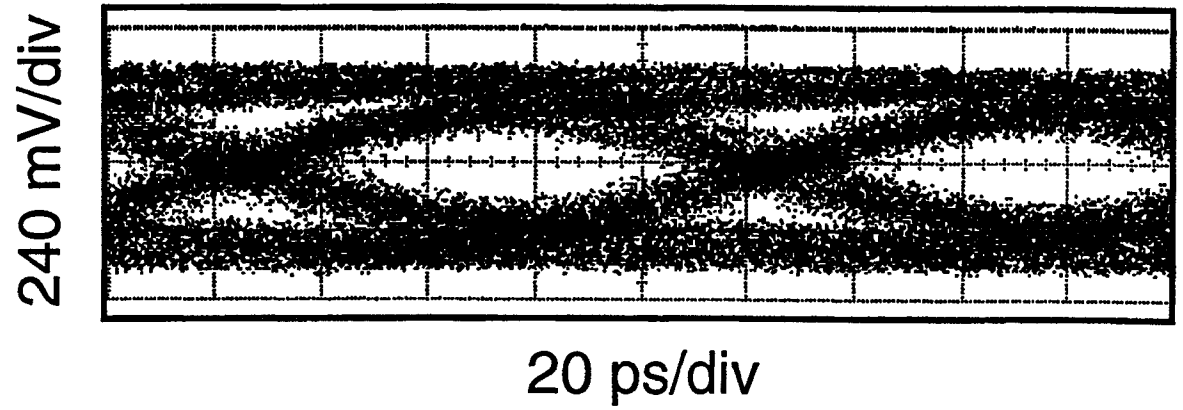
f_T doubler speeds up slow path to eliminate "flat-spot" in summed output

Eye Diagrams



Eye at package Pin

- 3ps (RMS) / 18ps (p-p)
- systematic jitter < 3ps (peak)

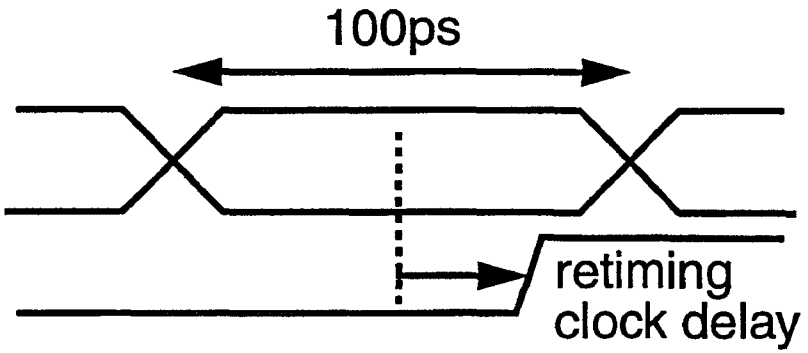


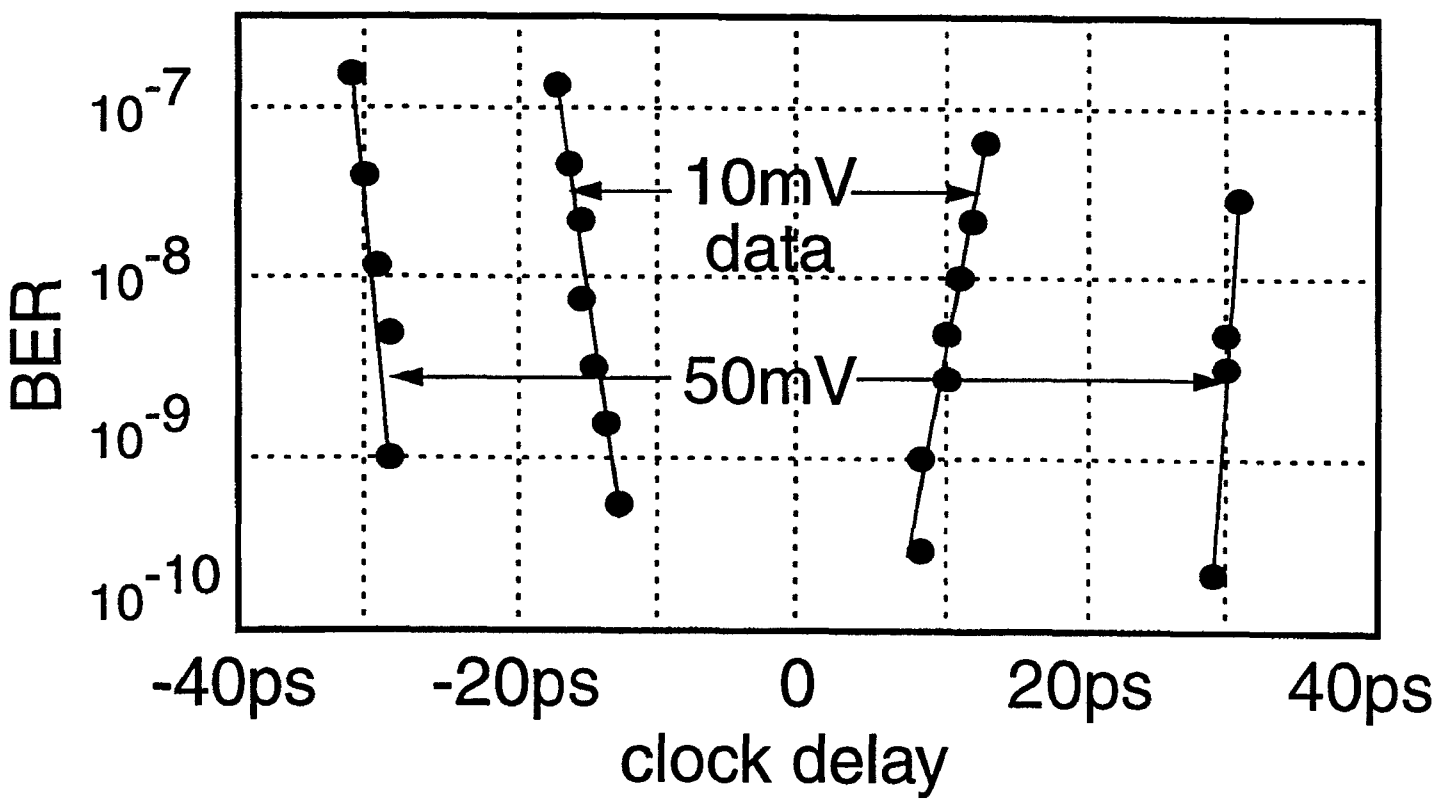
Eye after 21' of 0.19" coax

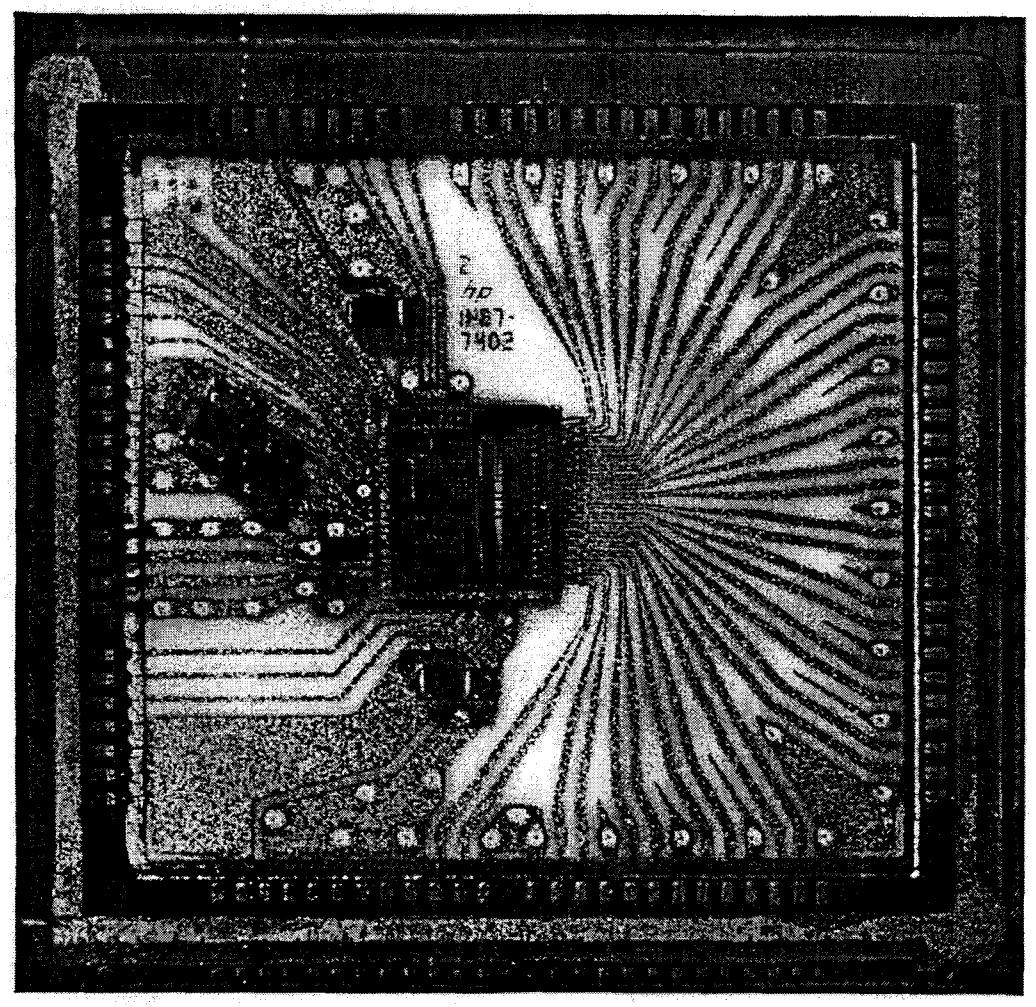
- BER < 10^{-14}

Receiver Eye Margin

("zero-length" coax)

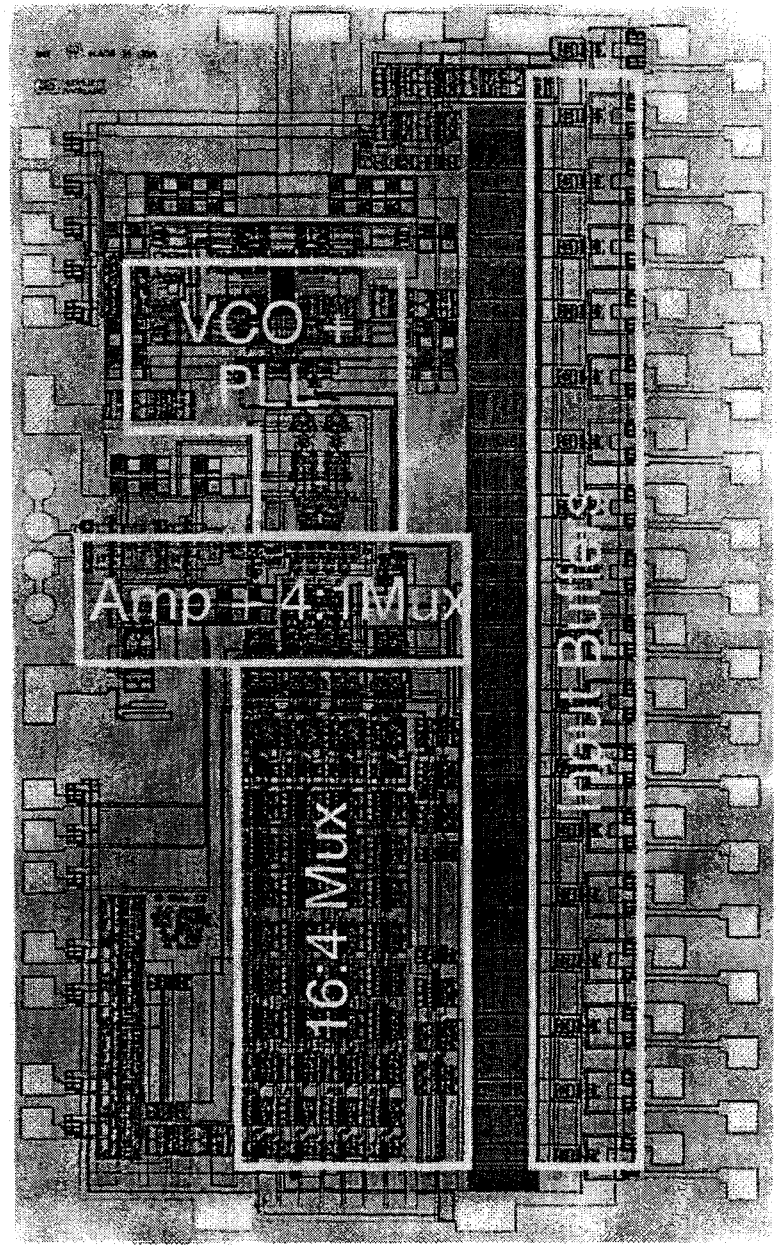






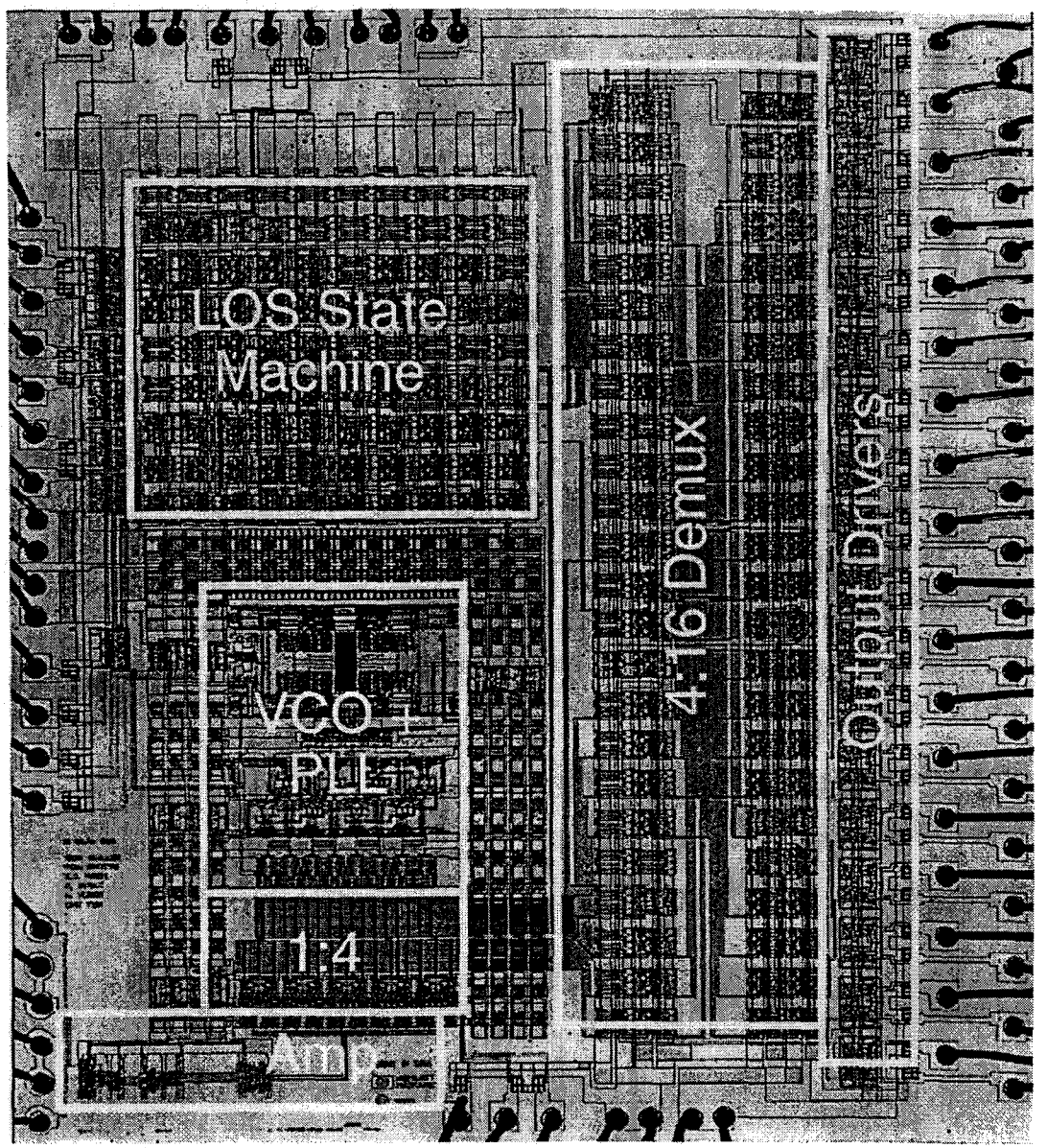
Packaging

- Custom 100-Pin Package
- Kovar Baseplate
- Ceramic Sidewall
- "Fine-line" alumina hybrid
- S_{11} better than 20dB to 5GHz, 15dB to 8GHz



TX Summary

- Die size: 2.6x4.4mm^2
- Power: 3.0W
- Supply: -5.2V
- ECL-style design in 25GHz f_T Si-Bipolar Process
- Output swing: 800mV p-p (doubly terminated)
- Output rise/fall: <40ps (20/80%) (package limited)



RX Summary

- Die size: 3.9x4.4mm^2
- Power: 5.0W
- Supply: -5.2V
- ECL-style design in 25GHz f_T Si-Bipolar Process
- Input sensitivity:10mV (BER < 10^{-14})

Conclusion

- Using Multi-phase sampling techniques, 10 Gb/s transmission is achieved with 25 GHz f_T Silicon Bipolar process.
- Good BER performance is achieved across 21 feet of Gore 0.19" coaxial cable.
- Chipset provides low-cost alternative to fiber-optic links for short connections in computer, router and instrument backplanes.