FP 15.5: A 2.488Gb/s Si-Bipolar Clock and Data Recovery IC with Robust Loss of Signal Detection

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SONET 2.488Gb/s transmission and switching systems, network backbones, and video transmission are among the many application areas benefiting from inexpensive and robust clock and data recovery circuits (CDR). Previous commercial solutions have required multiple chips and GaAs processes to perform this function [1]. This 25GHz f_T Si-Bipolar chip operates from 2 to 3Gb/s over worst-case process, temperature and voltage variations, dissipating 1.77W from 5V ±10% supply, requiring a single off-chip filter capacitor [2]. For network monitoring, a loss-of-signal (LOS) detector operates on phase-error events, with a trigger threshold programmable between 10^{-4} and 10^{-6} BER.

A simplified block diagram of the chip is shown in Figure 1. The inputs are ac-coupled, driven either single-ended or differentially. A Cherry-Hooper wideband amplifier is used to minimize pulsewidth distortion with single-ended input signals [3]. The phase-locked-loop portion of the circuit includes two different phase detector blocks. The first phase/frequency detector (FDET) initially trains the VCO to the desired bit frequency using an external low-frequency reference, and asserts the frequency-lock signal (flock) when successful. The second phase detector (PDET) produces three signals: data transition detect (dtrans), data lock detect (dlock), and a tri-state bang-bang phase-error signal. Once the VCO is frequency locked to the reference, and data transitions are present, the PLL is switched to the bang-bang phase detector. If the data lock detector stabilizes within a certain time, then the loop remains locked to the data, otherwise the VCO is retrained to the reference clock and the sequence repeats.

Data-lock is lost whenever the VCO is retrained to the reference clock, so the LOS algorithm must be extremely reliable. The LOS algorithm uses information from a data lock detector that operates by monitoring the location of the data zero-crossings. Transitions occurring more than ±135° away from the nominal location are flagged as a raw phase errors (PE). The nominal design target is that the link should have a mean time to restart (MTTR) of less than 1/10 second at 10^{-5} BER, and greater than a year at 10^{-7} BER. If the link were simply restarted on isolated PE events, there would be a 1:1 relationship between BER and MTTR. To achieve an MTTR > 1 year would then require a BER of 10^{-16}! A way to steepen the LOS/BER relationship is to process PE events in multi-bit "bins", requiring multiple consecutive bins to each contain at least one error before asserting LOS. The current design groups PE events into bins of size N, requiring M consecutive errored bins before asserting LOS. Assuming that the phase error rate is approximately equal to half the BER, then

$$MTRR \approx \frac{N \bullet t_{bit}}{\left(1-\left(1-\frac{BER}{2}\right)^{N}\right)^{M}}$$

The exponent M in the denominator sets the slope relation between PE and MTTR. With M=7, only about 1 decade change in BER is needed to change MTTR from 1 second to 1 year. Four different LOS thresholds between approximately 10^{-4} and 10^{-6} BER are selectable by bond-options. The exact BER varies according to the application due to the system-dependent relationship between PER and BER. Figure 3 shows measured versus calculated MTTR for a system in which M=7, and $N=2^{16}$.

The PLL uses a bang-bang phase detector and positive-feedback charge pump similar to those described in Reference 4. The VCO is composed of a cascade of 2 variable-delay blocks as shown in Figure 4. Each variable-delay block is composed of two interpolation sections to extend the tuning range while minimizing interpolation jitter. Outputs are taken from non-critical nodes to minimize loading. The main tuning input is prefiltered by two 100MHz poles to reduce sensitivity to power supply noise. The wide-bandwidth bang-bang tuning input has 500 times less gain than the main tuning input, and is implemented by injecting small currents into the interpolation cell.

The two-tuning-input VCO architecture, in conjunction with a binary-quantized phase detector, results in a VCO drive voltage equivalent to a first-order ΣΔ conversion of the loop frequency error. The ability of the loop to track incoming phase jitter is a slew-rate-limited process, with an effective jitter bandwidth proportional to jitter amplitude. In practice, this is ideal behavior for the input of a SONET regenerator, where a wide jitter-tracking bandwidth minimizes sampling errors, and where the overall system jitter transfer function will be set by a separate narrow-band transmitter PLL. For this design, the bang-bang amplitude and charge pump time constant have been set to meet the SONET jitter-tolerance specification. The resulting jitter generation, as calculated from the jitter spectrum in Figure 5, is 0.0049UI RMS. Figure 6 shows the time-domain PLL operation in the presence of noisy data. Figure 7 is a chip micrograph. The layout uses a gate-array methodology with fully-differential ECL cells and 3606 active devices (less than ½ of the array capacity).

Acknowledgments:

The authors thank S-Y. Chai, J. Norman, T. Goh, and L. Dove for help in development.

References:

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[2] Huang, W., et al., "A high-speed bipolar technology featuring self-aligned single-poly base and submicrometer emitter contacts," IEEE Electron Device Letters., vol. 11, no. 9, pp. 412-414, Sept., 1990.

[3] Faulkner, D., "A Wide-Band Limiting Amplifier for Optical Fiber Repeaters," IEEE Journal of Solid State Circuits, vol.18, no.3, pp. 333-340, June, 1983.

[4] Lai, B., R. C. Walker, "A Monolithic 622Mb/s Clock Extraction Data Retiming Circuit," ISSCC Digest of Technical Papers, pp.144-145, Feb., 1991.

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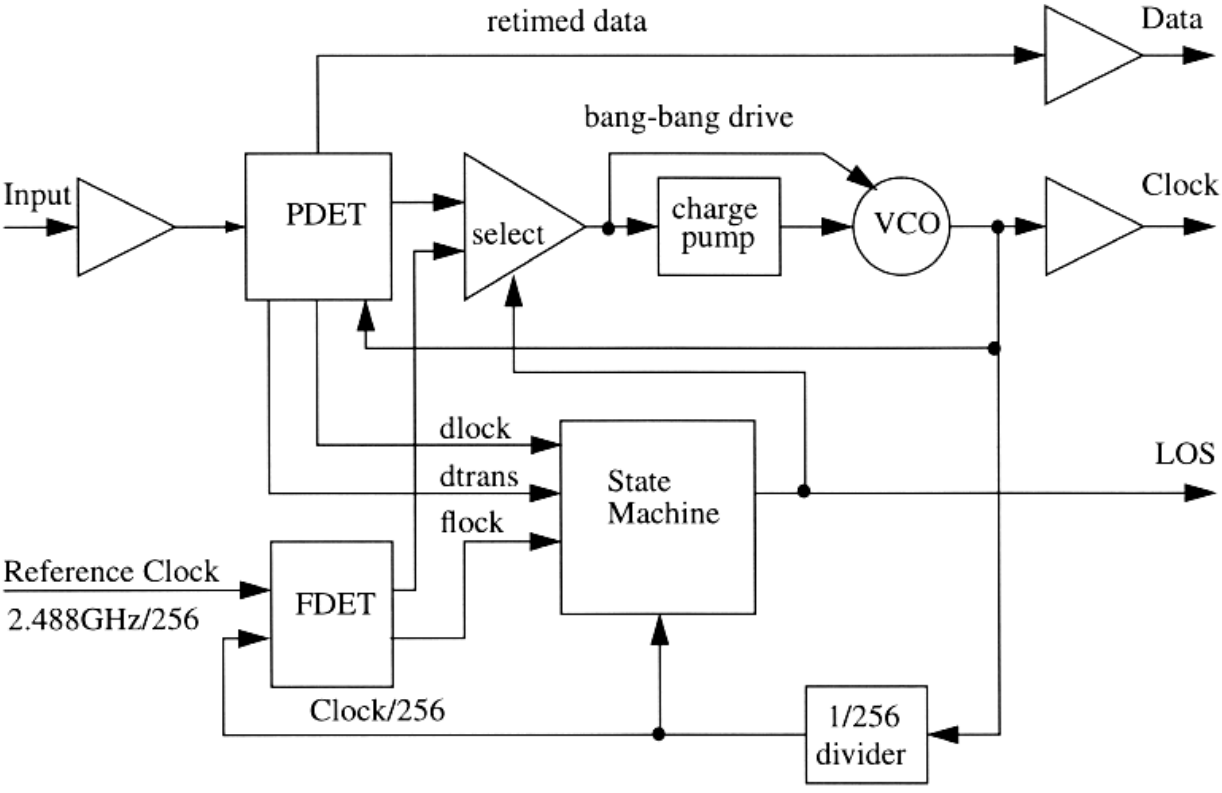
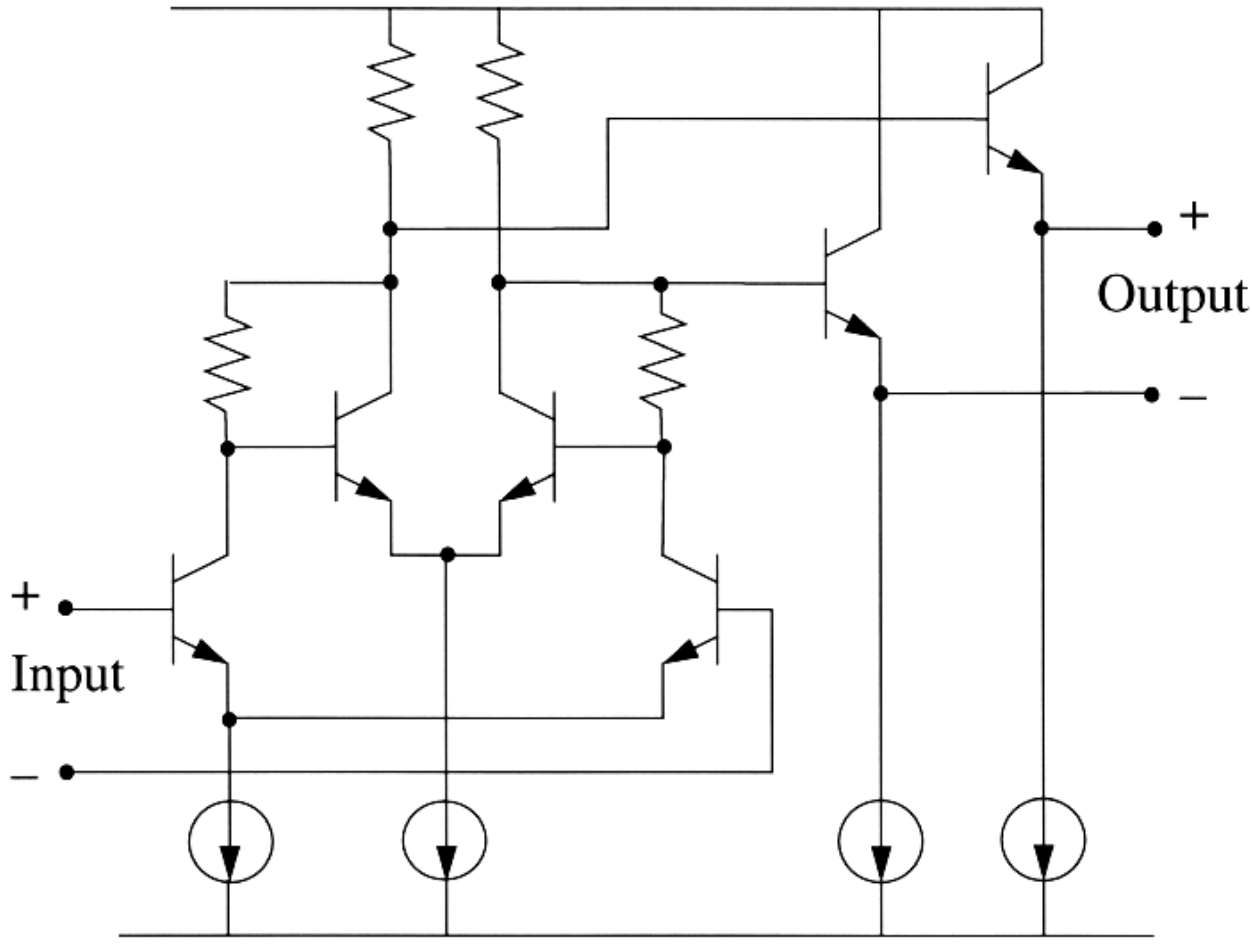
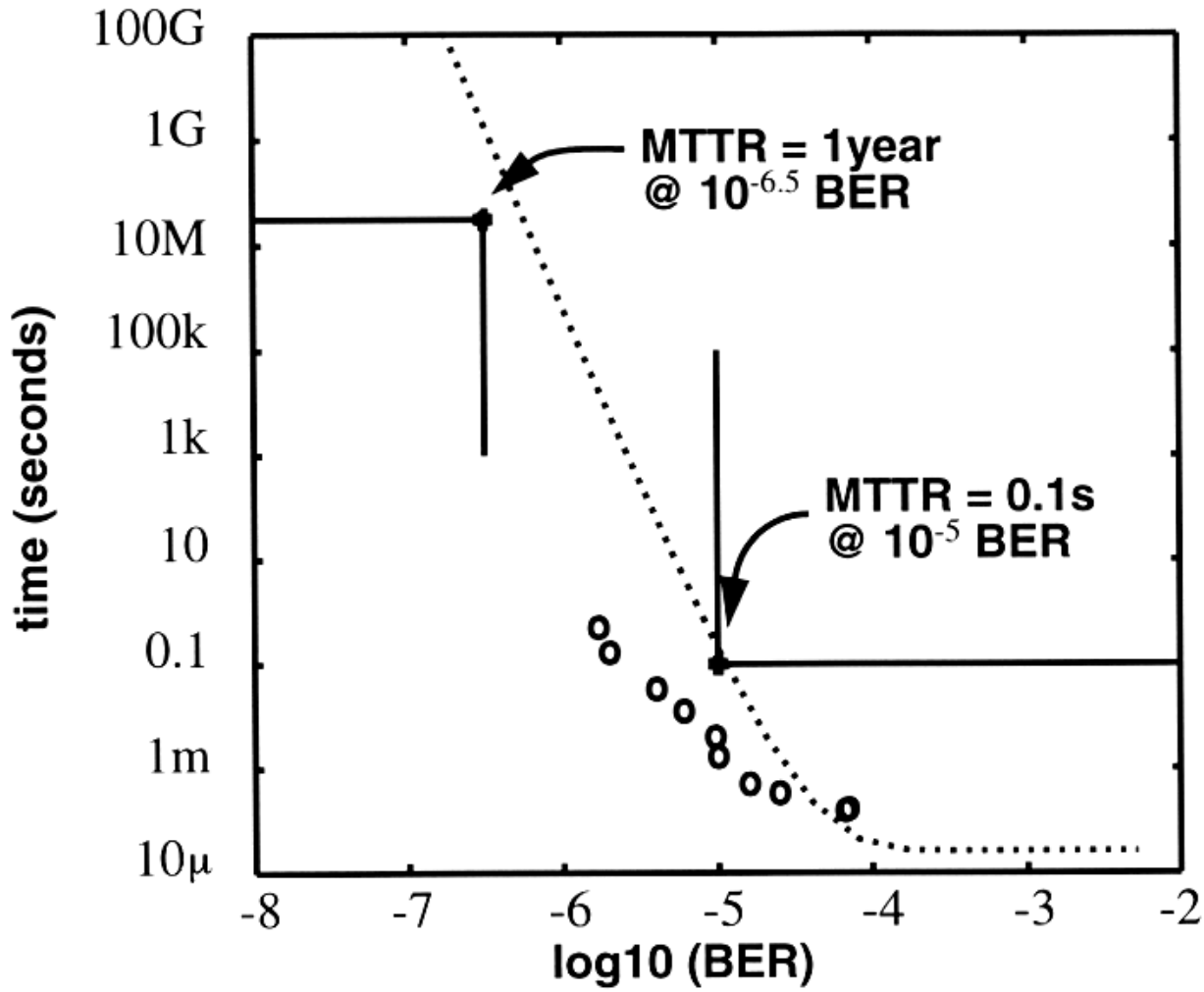


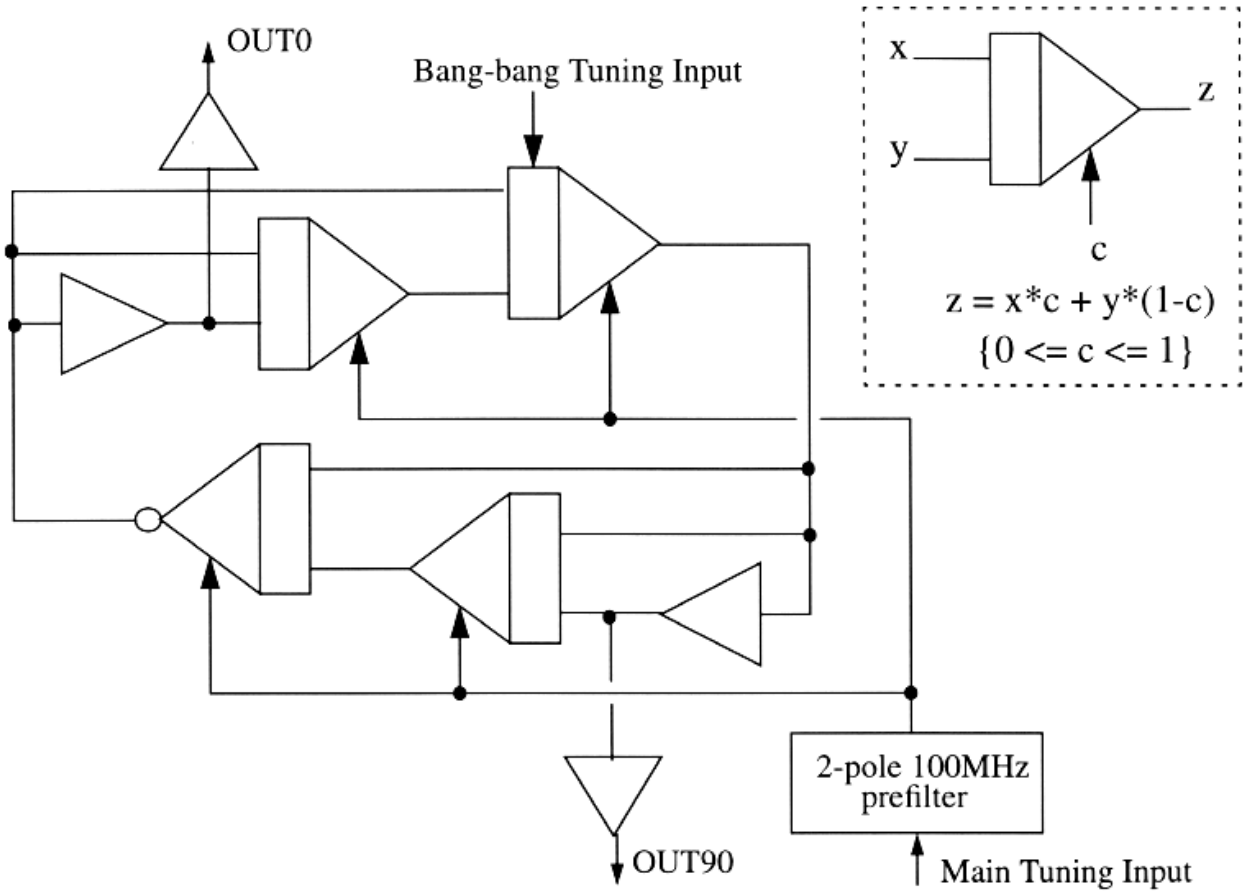
15-5-1: Overall chip block diagram.



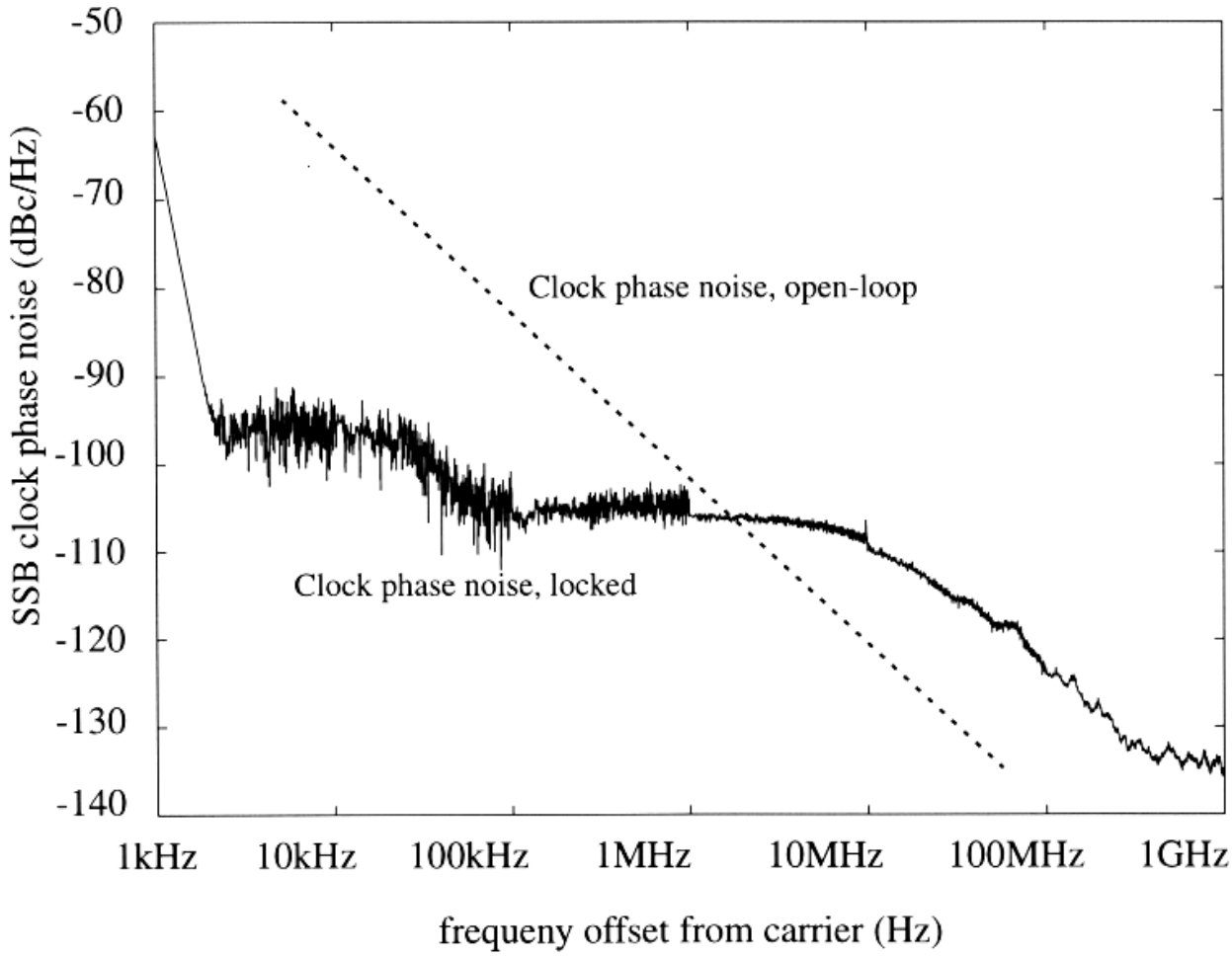
15-5-2: Data input buffer.



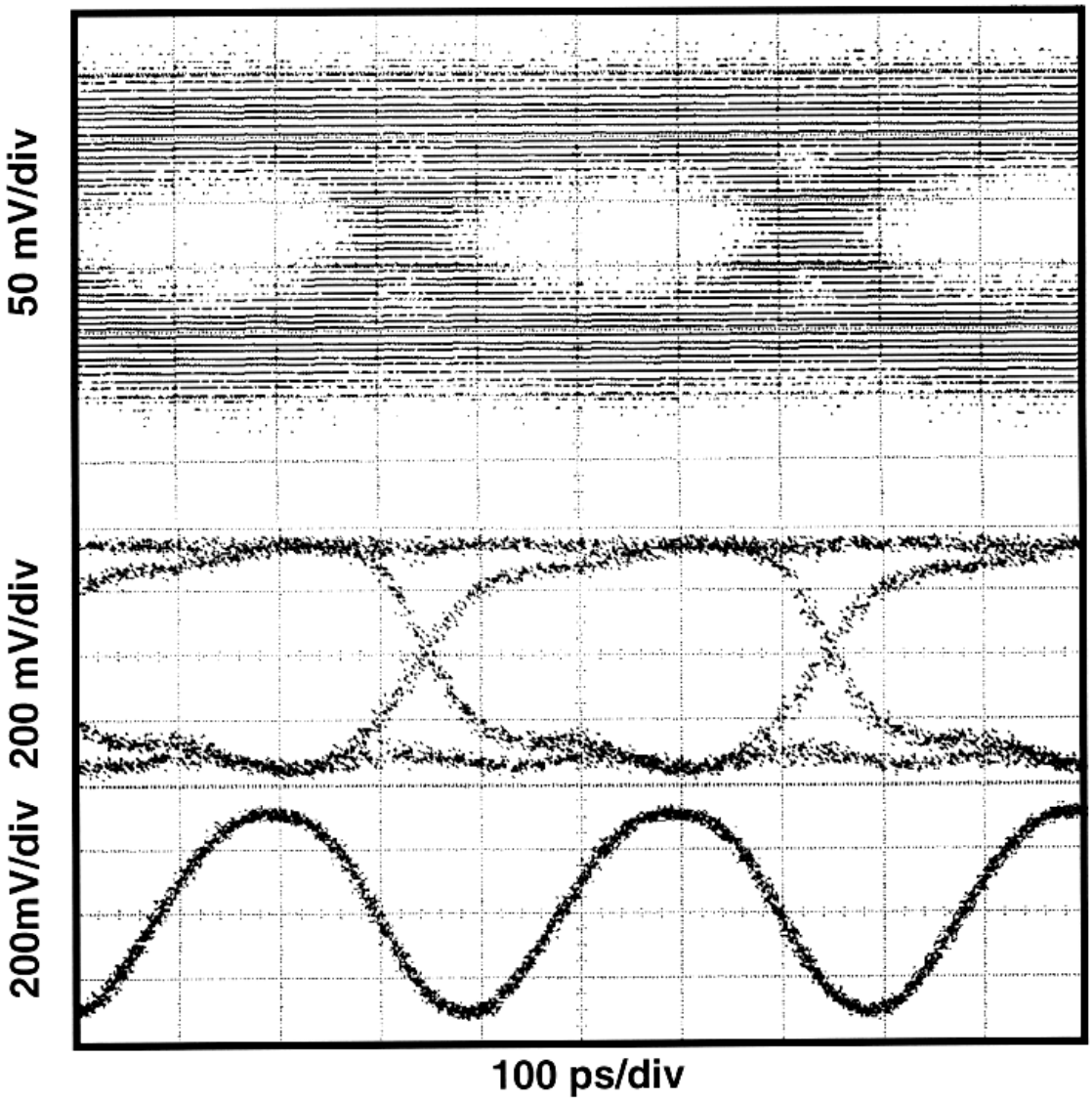
15-5-3: Calculated and measured mean time to restart vs. BER. The circles are measured data points.



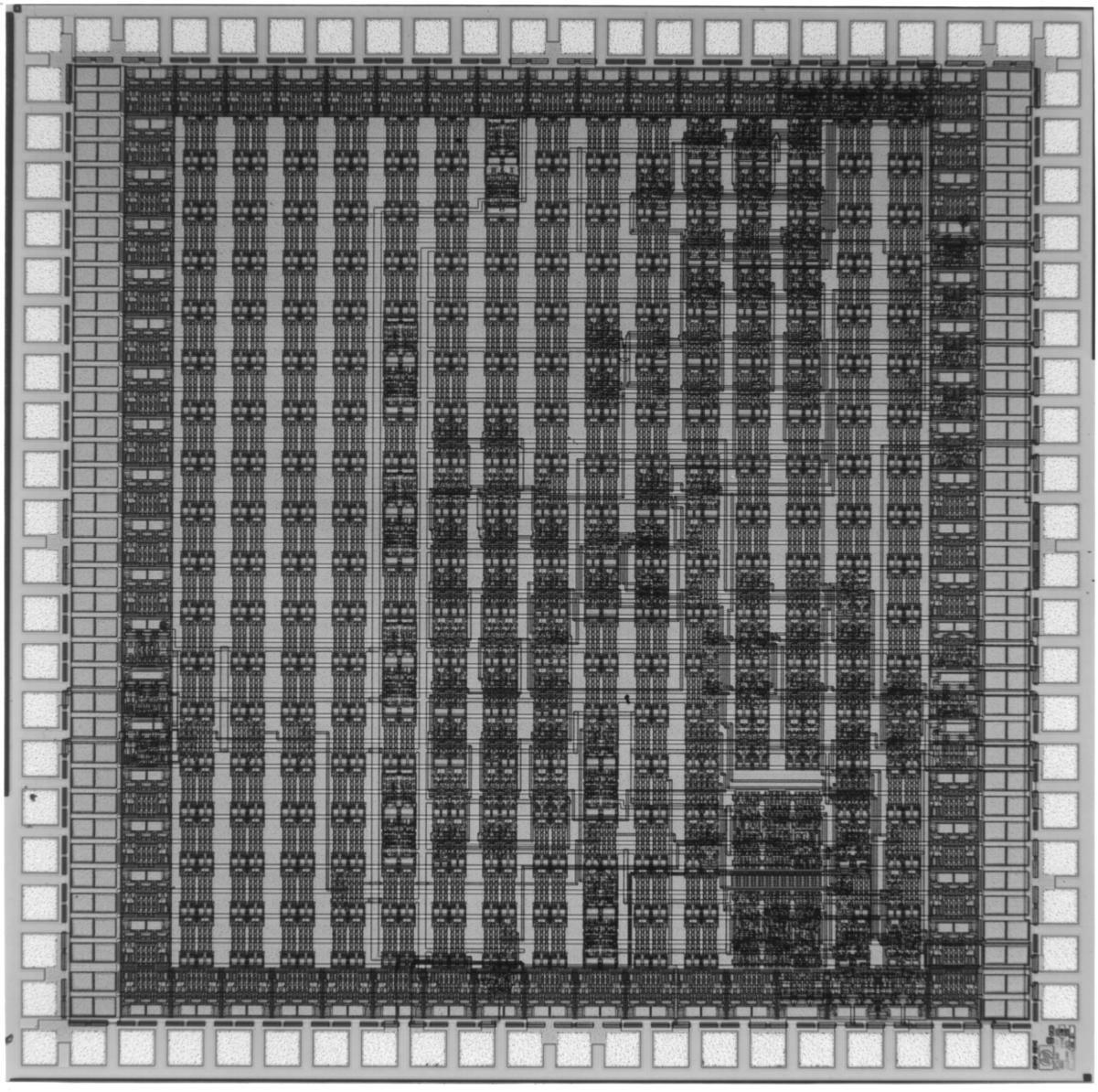
15-5-4: VCO block diagram showing cascaded mixer cells.



15-5-5: Clock SSB phase noise measured open-loop and locked to 2^{23}-1 PRBS sequence.



15-5-6: Top trace: Input 2^{23}-1 PRBS data with broad band noise added to achieve 10^{-4} BER. Middle trace: Recovered data eye. Bottom trace: Recovered clock. All signals triggered off of BERT clock.



15-5-7: Micrograph of 3.45x3.45mm² clock and data recovery die.