Clock and Data Recovery for Serial Digital Communication

focusing on bang-bang loop CDR design methodology

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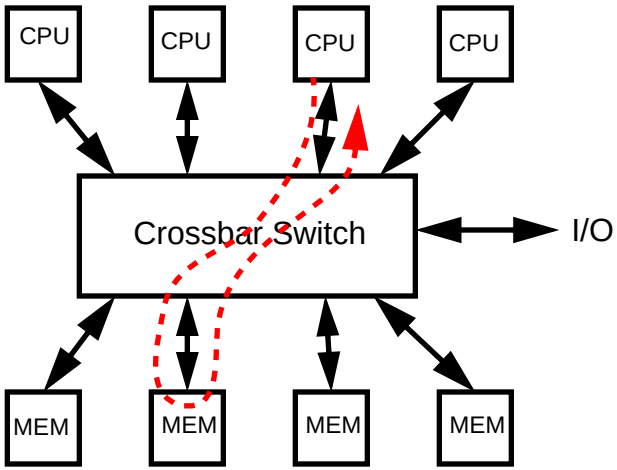
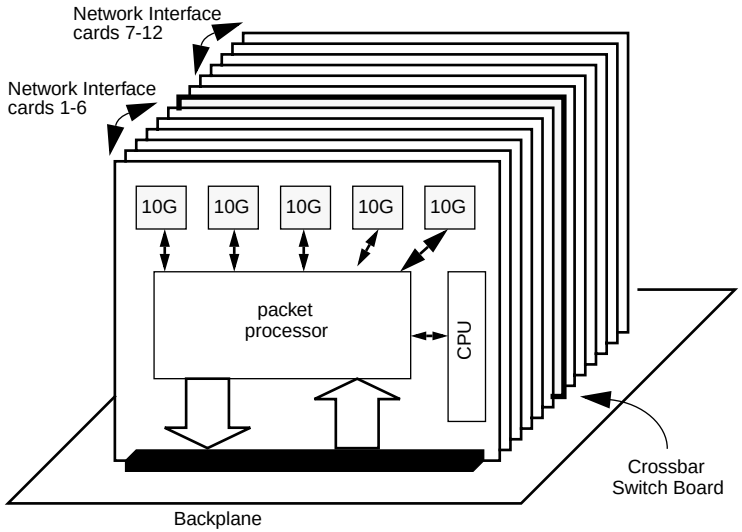
Outline

- Overview of serial data communications
  - Degradation mechanisms, data coding
  - Jitter measurements
- Clock recovery methods
  - Linear PLL review and components
  - BB PLL theory

Diversity of CDR applications



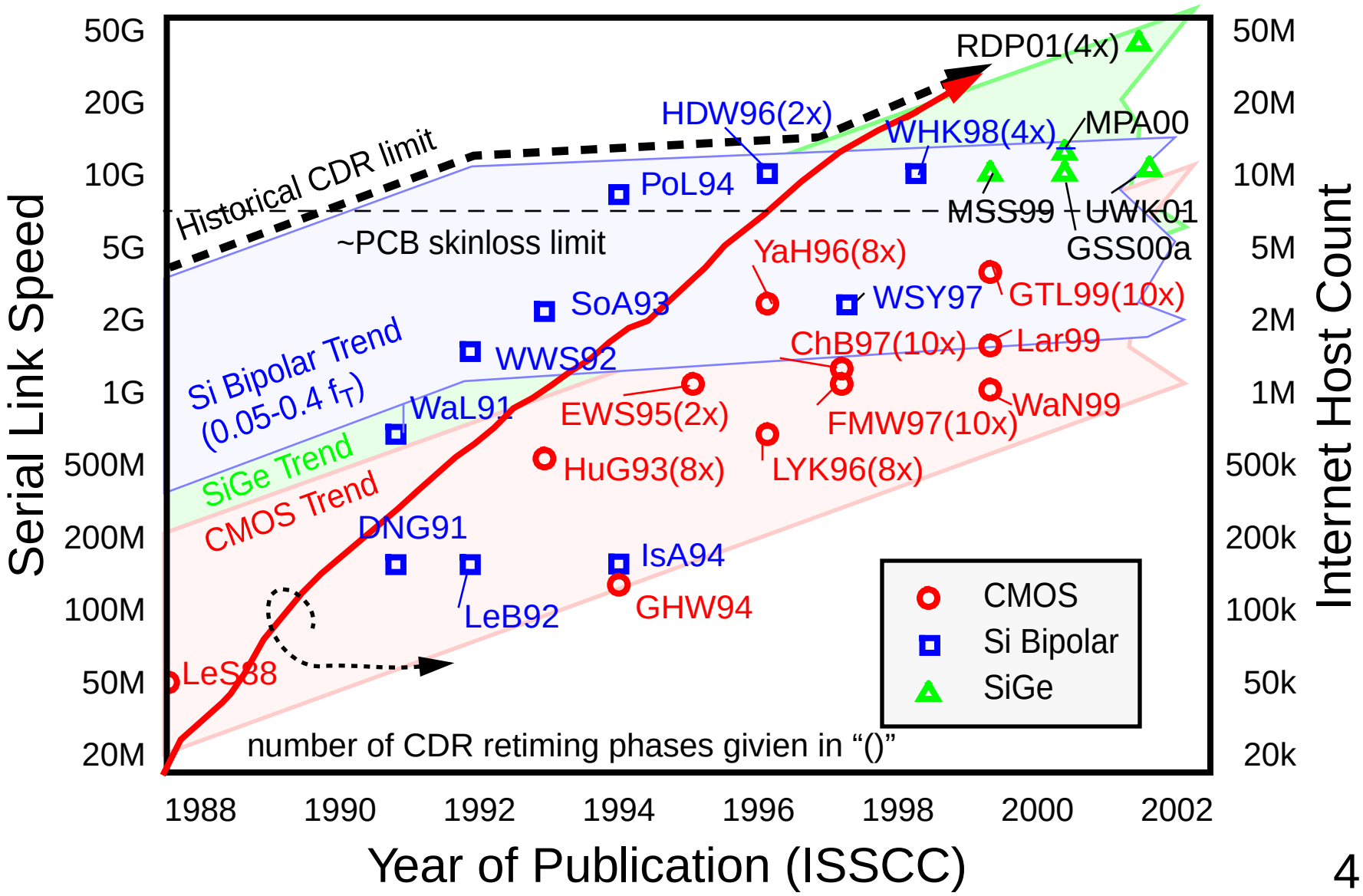
Linecard to Router



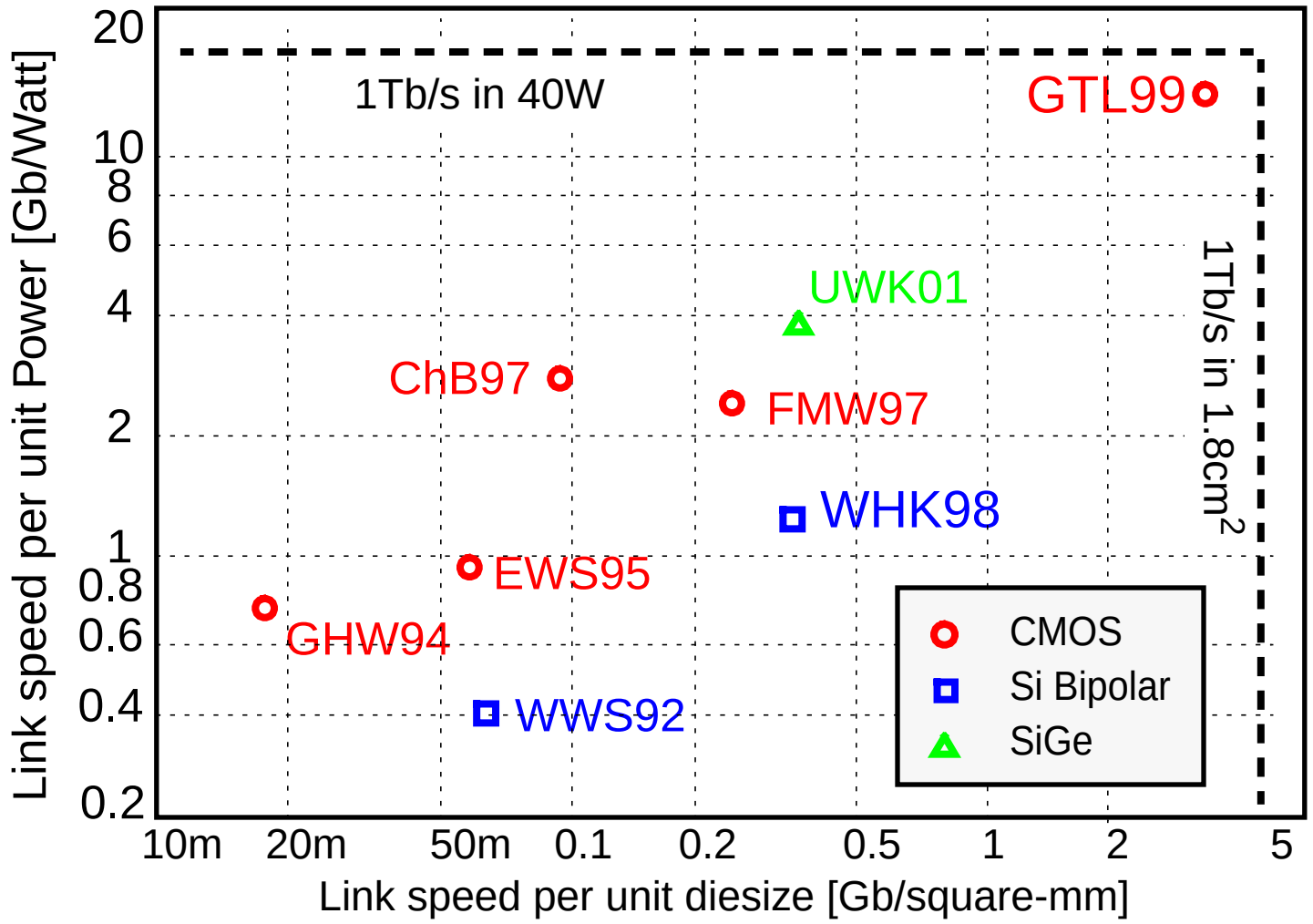
CPU-CPU/Memory

- Clock and Data Recovery applications span the range from high-volume, low-cost datacom applications to high-performance, long-haul telecom applications
- Many different trade-offs tailor each circuit to the target

CDR data rates over time



TX/RX Gb/W and Gb/mm^2

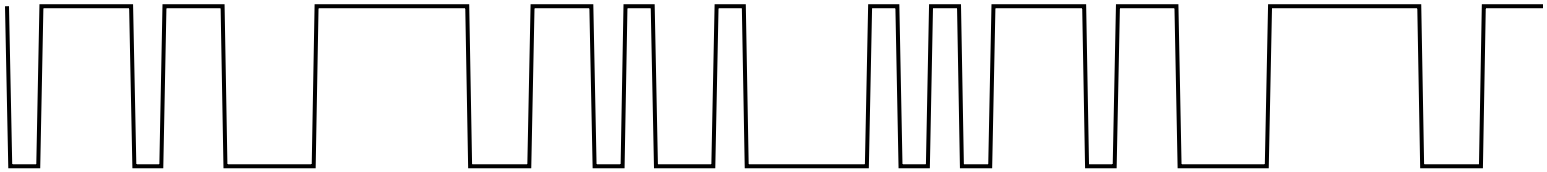


Circuit power and die size can be system-limiting factors. Gb/W and Gb/mm^2 are plotted for complete TX/RX designs published between ISSCC'92 and 2001. Dashed lines represent an agressive chip supporting 1Tb/s in a total of 40W and 1.8cm^2.

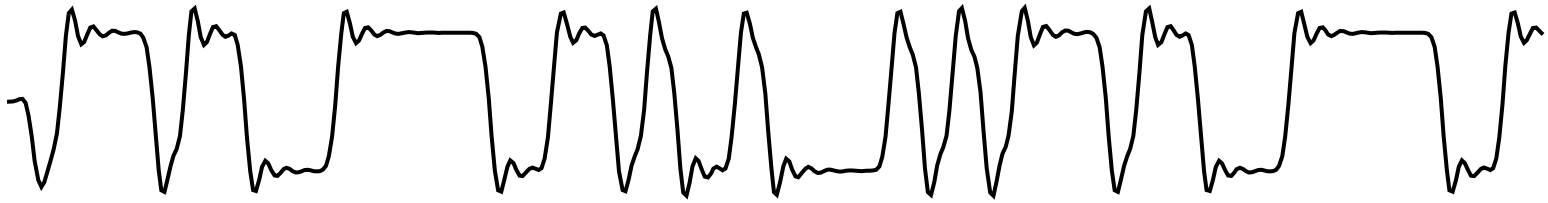
Basic Idea

Serial data transmission sends binary bits of information as a series of optical or electrical pulses:

01110110001111100110100100001010111011000111111..



The transmission channel (coax, radio, fiber) generally distorts the signal in various ways:



From this signal we must recover both clock and data

Some Signal Degradation Mechanisms

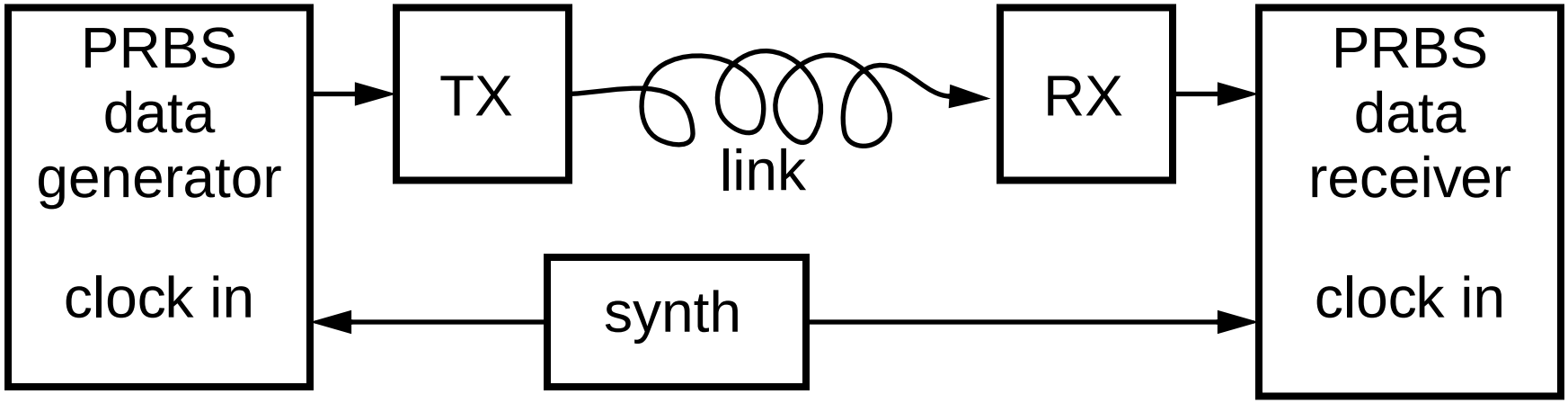
- AC coupling droop, baseline wander
- Optical pulse dispersion
- Skin / dielectric loss [YFW82, WWS92, FMW97]
- Random noise
- E+O crosstalk
- Intersymbol interference
- Connector discontinuities

Coding for Desirable Properties

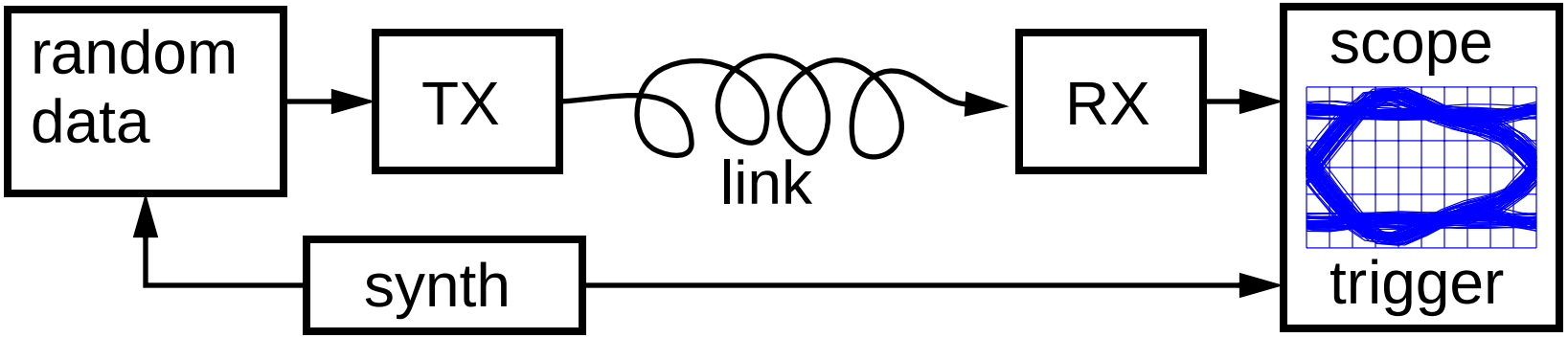
- DC balance, low disparity
- Bounded run length
- High Coding Efficiency
- Spectral Shaping (eg: reduce BW or DC component)
- *Many Variations are Possible!*
  - Manchester [San82]
  - mB/nB [Gri69][Rou76][WiF83] [YKI84] [Pet88]
  - Scrambling: SONET, 64b/66b [CCI90]
  - CIMT [WHY91], Conservative Code [Ofe89]

Bit Error Rate (BER) Testing

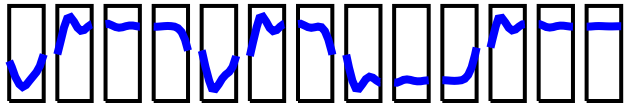
- Pseudo-Random-Bit-Sequence (PRBS) is used to simulate random data for transmission across the link
- PRBS pattern 2^N-1 Bits long contains *all* N-bit patterns
- Number of errored-bits divided by total bits = BER.
- Typical links are designed for BERs better than 10^{-12}



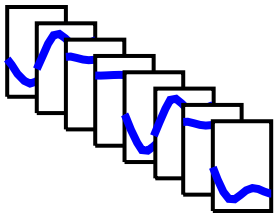
Eye diagram construction

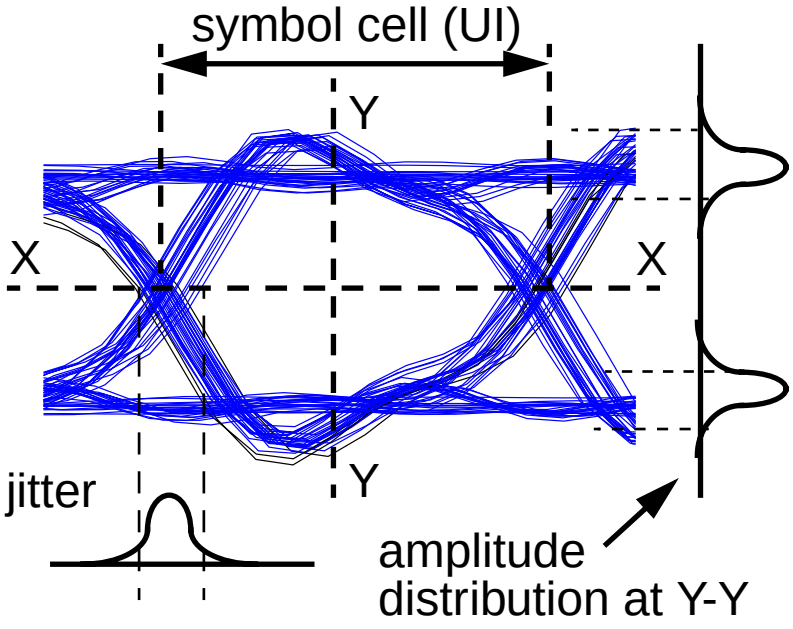


Use a precise clock to chop the data into equal periods

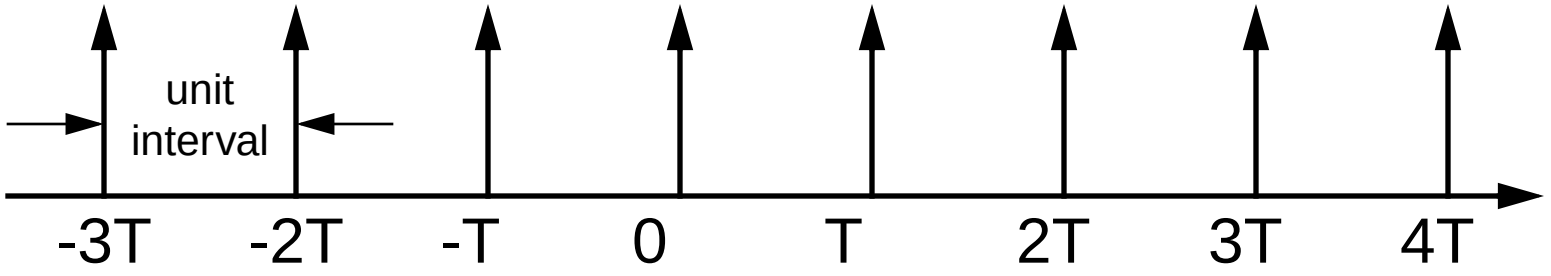


overlay each period onto one plot

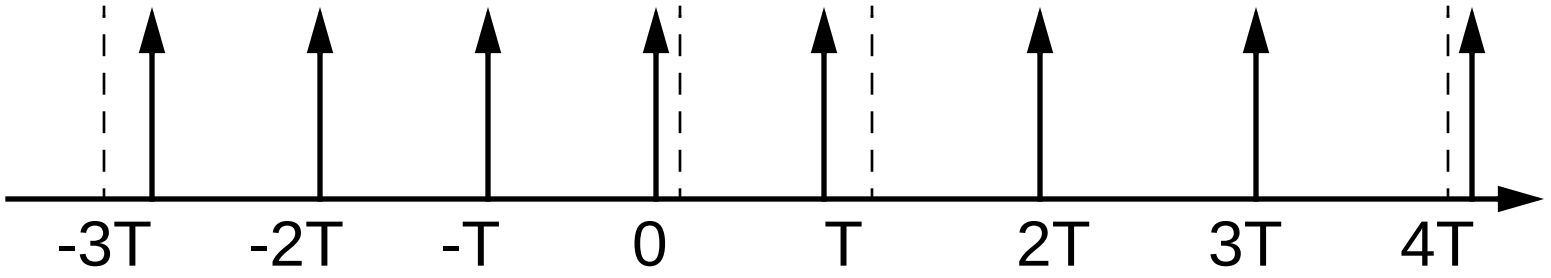




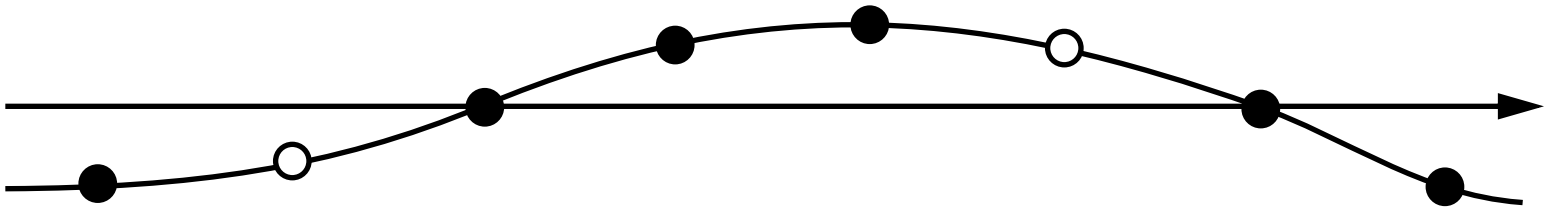
Definition of Jitter



Impulses spaced equally in time (jitter free signal)



Impulses spaced irregularly in time (jittered signal)



Errors treated as discrete samples of continuous time jitter

After Trischitta and Varma: “Jitter in Digital Transmission Systems”

Jitter Measurements

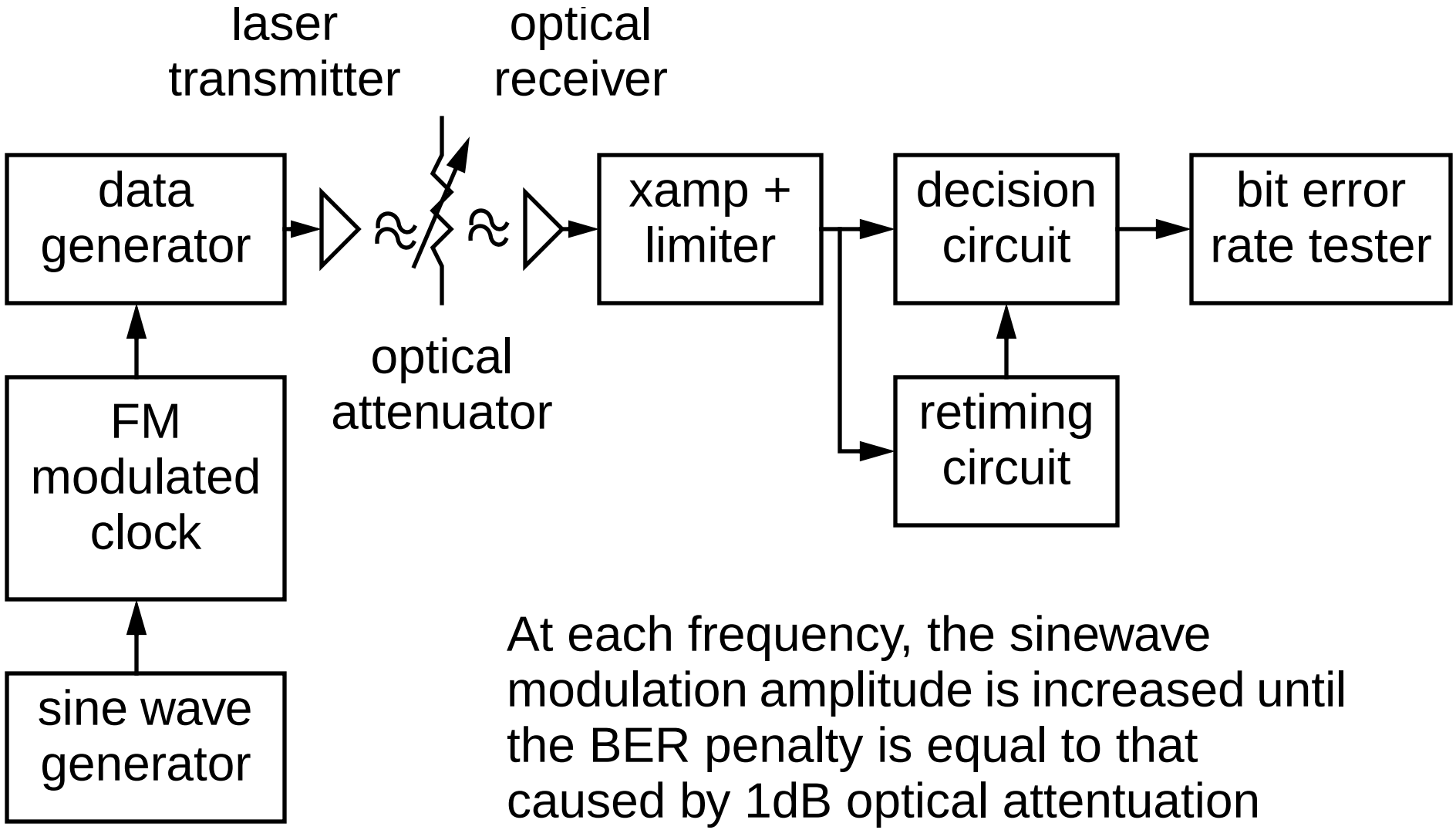
Jitter Measurements

- *Datacom Style:* Ethernet + Fiber Channel
  based on time-domain eye diagrams
  - Deterministic Jitter
  - Random Jitter
- *Telecom Style:* SONET
  based on frequency-domain jitter spectrums
  - Jitter Tolerance
  - Jitter Transfer
  - Jitter Generation

Deterministic and Random Jitter

- Random Jitter (RJ)
  - data source is simple repetitive “clock-like” pattern.
  - RMS jitter is measured at zero crossings of eye-diagram
  - measured jitter is mostly due to clock noise
- Deterministic Jitter (DJ)
  - data source is complex scrambled data
  - pk/pk jitter is measured at zero crossings of eye-diagram
  - RJ contribution is subtracted from the measurement
  - measured jitter is mostly due to bandwidth limitations in the data path.

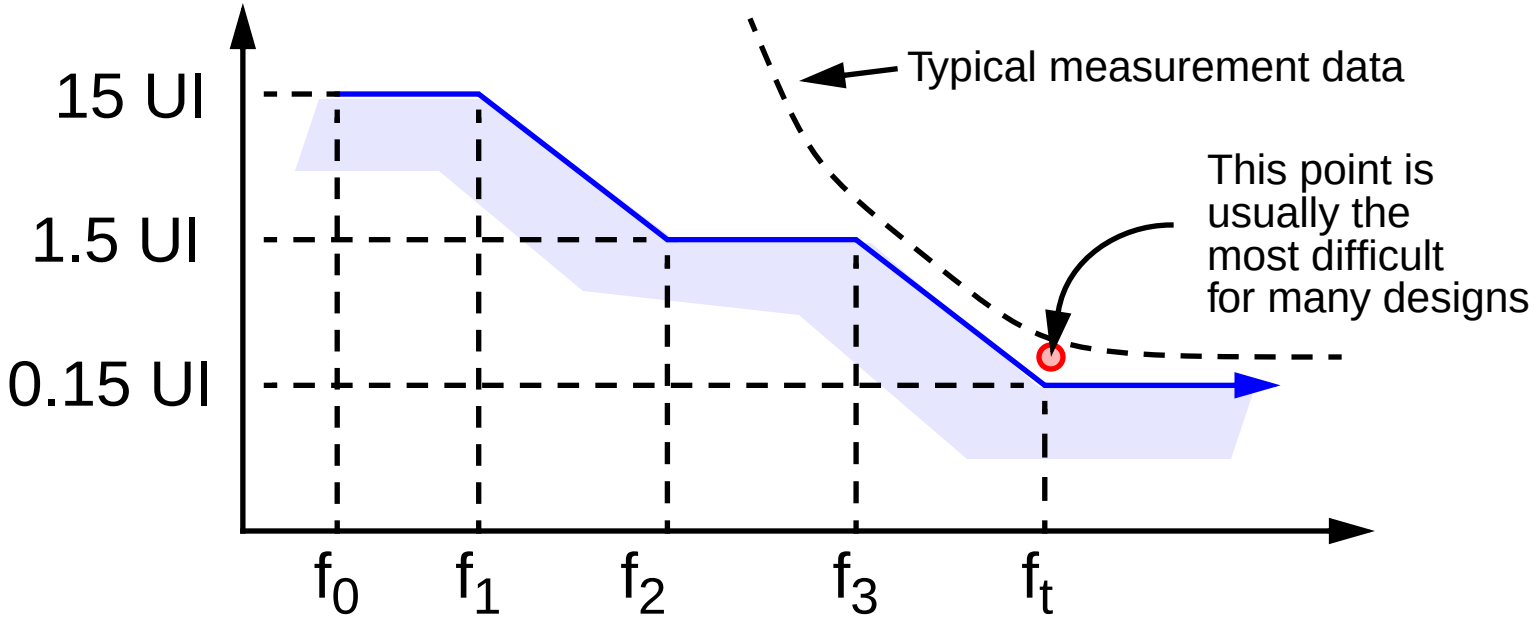
Jitter Tolerance Test Setup



At each frequency, the sinewave modulation amplitude is increased until the BER penalty is equal to that caused by 1dB optical attentuation

After Trischitta and Varma: “Jitter in Digital Transmission Systems”

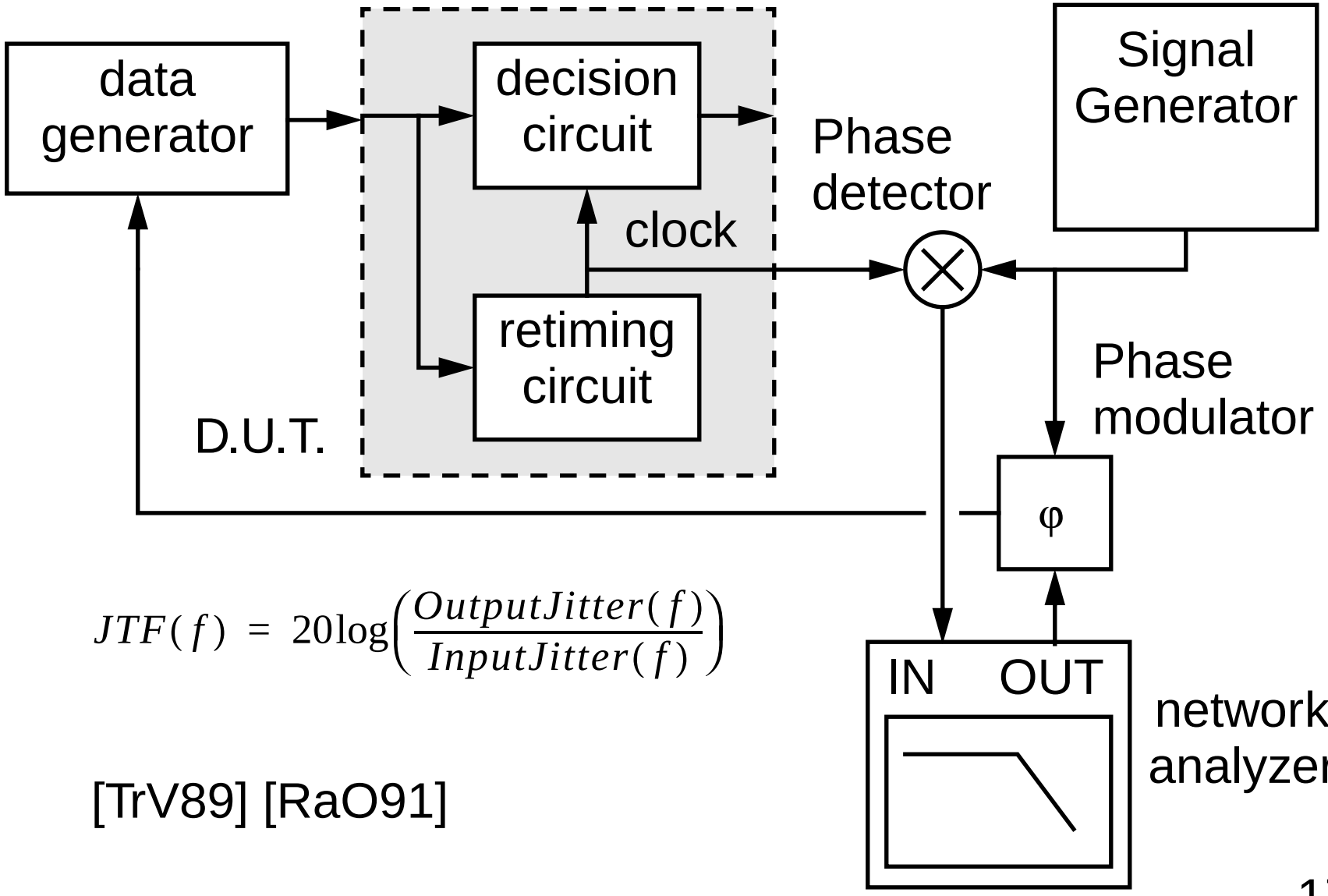
SONET Jitter Tolerance Mask



Data Rate		f_0[Hz]	f_1[Hz]	f_2 [Hz]	f_3 [kHz]	f_t [kHz]
OC-3	155 Mb	10	30	300	6.5	65
OC-12	622 Mb	10	30	300	25	250
OC-48	2.488 Gb	10	600	6000	100	1000
OC-192	10 Gb	10	2400	24000	400	4000

from SONET SPEC: TA-NWT-000253 Issue 6, Sept. 1990, fig 5-13

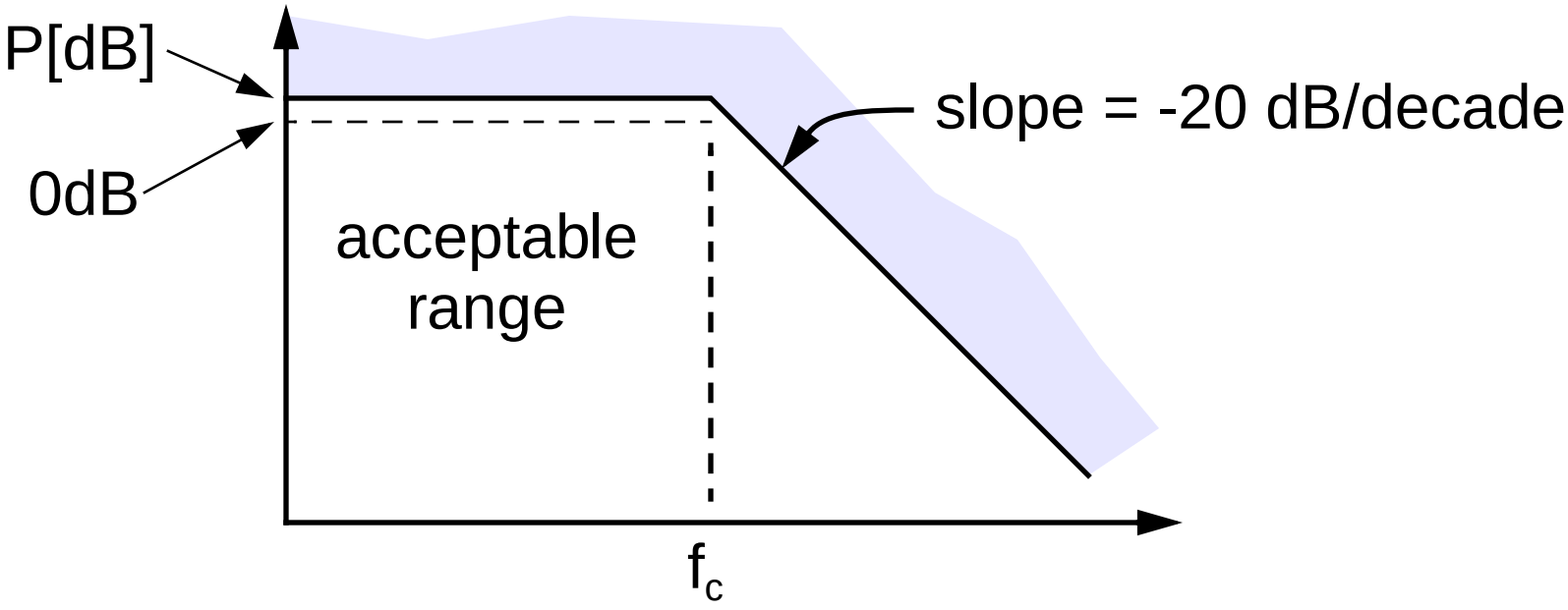
Jitter Transfer Measurement



$$JTF(f) = 20\log\left(\frac{OutputJitter(f)}{InputJitter(f)}\right)$$

[TrV89] [RaO91]

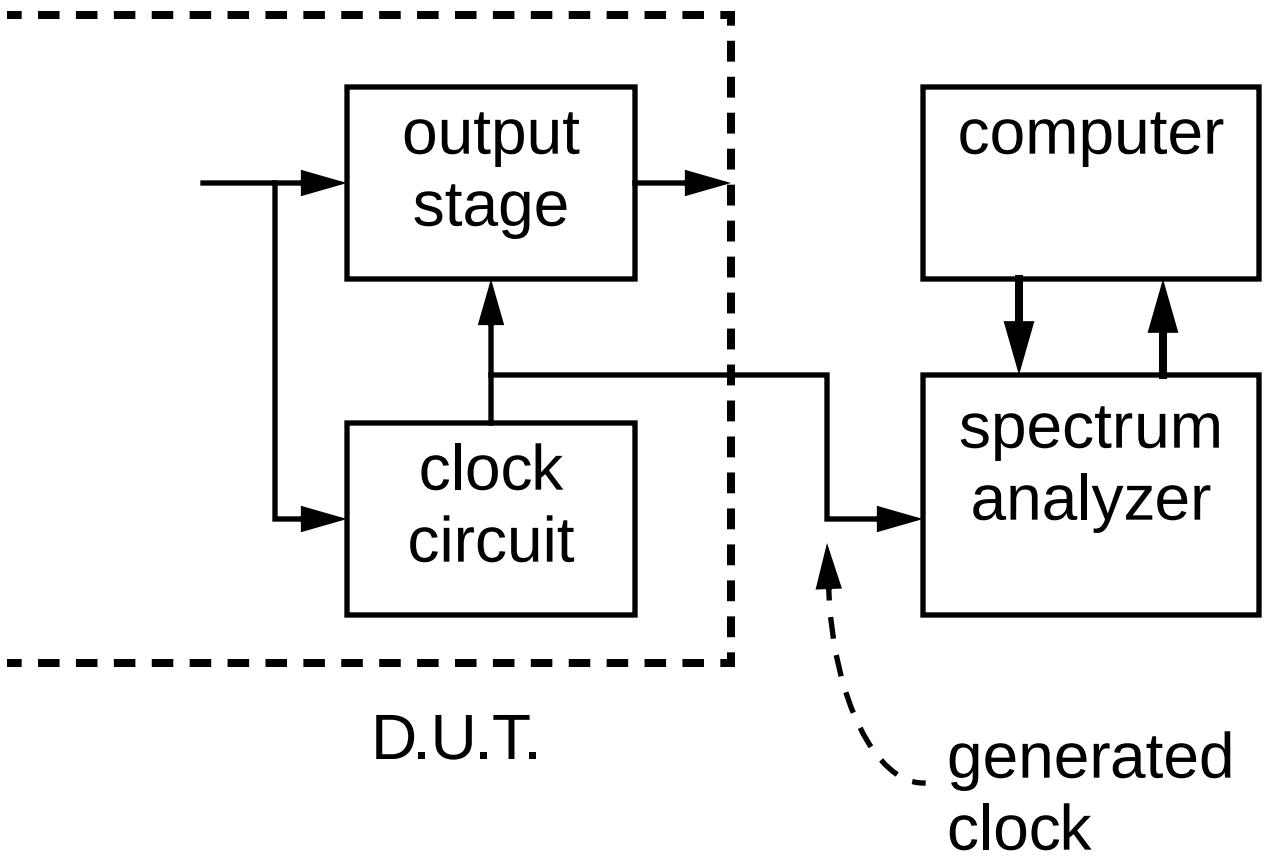
Jitter Transfer Specification



Data Rate	f_C[kHz]	P[dB]
155 Mb	130	0.1
622 Mb	500	0.1
2.488 Gb	2000	0.1

This specification is intended to control jitter peaking in long repeater chains

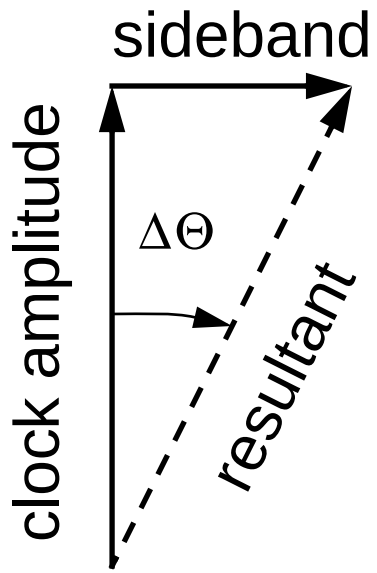
Jitter Generation



Jitter Generation (cont.)

1) Measure Jitter Sidebands around Clock

$$Jitter_{pp(rads)} = 2\Delta\Theta \cong 2\,\mathrm{atan}\left(\frac{V_{sideband}}{V_{clock}}\right)$$



2) Multiply Jitter components by Filter Mask

3) RMS sum total noise voltages over band

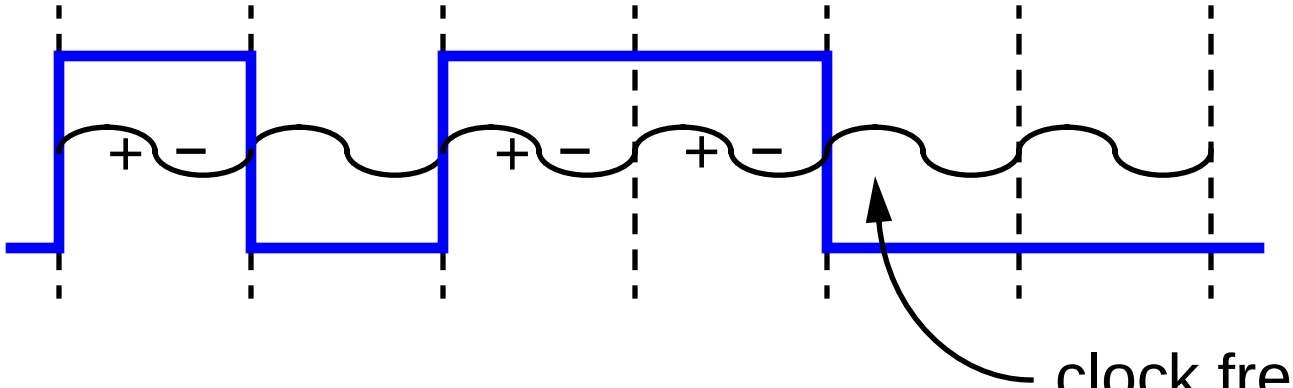
4) Convert RMS noise voltage to RMS jitter

OC-48 (2.488 Gb/s SONET) specifies 12 kHz hipass filter, and maximum 0.01 UI RMS integrated jitter.

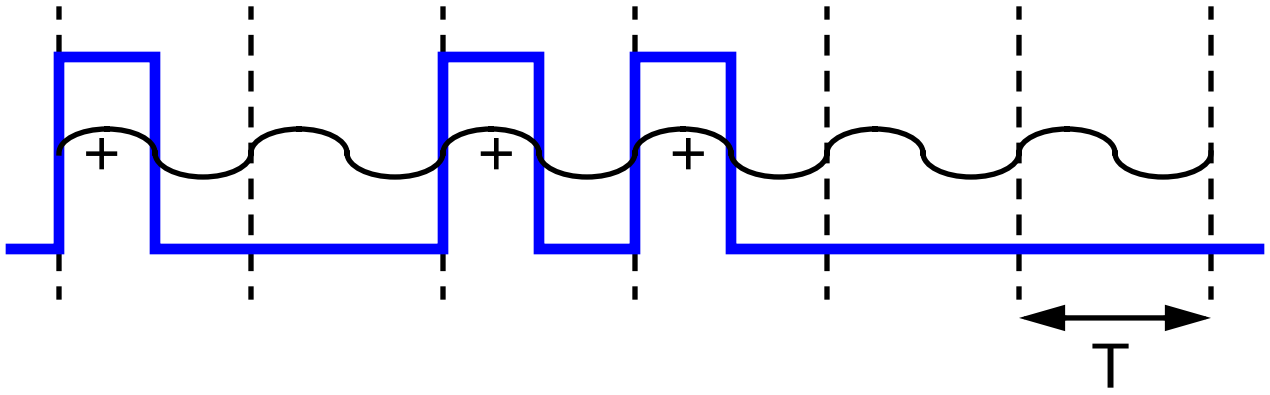
Clock Recovery Concepts

NRZ and RZ signalling

NRZ = “non return to zero” data

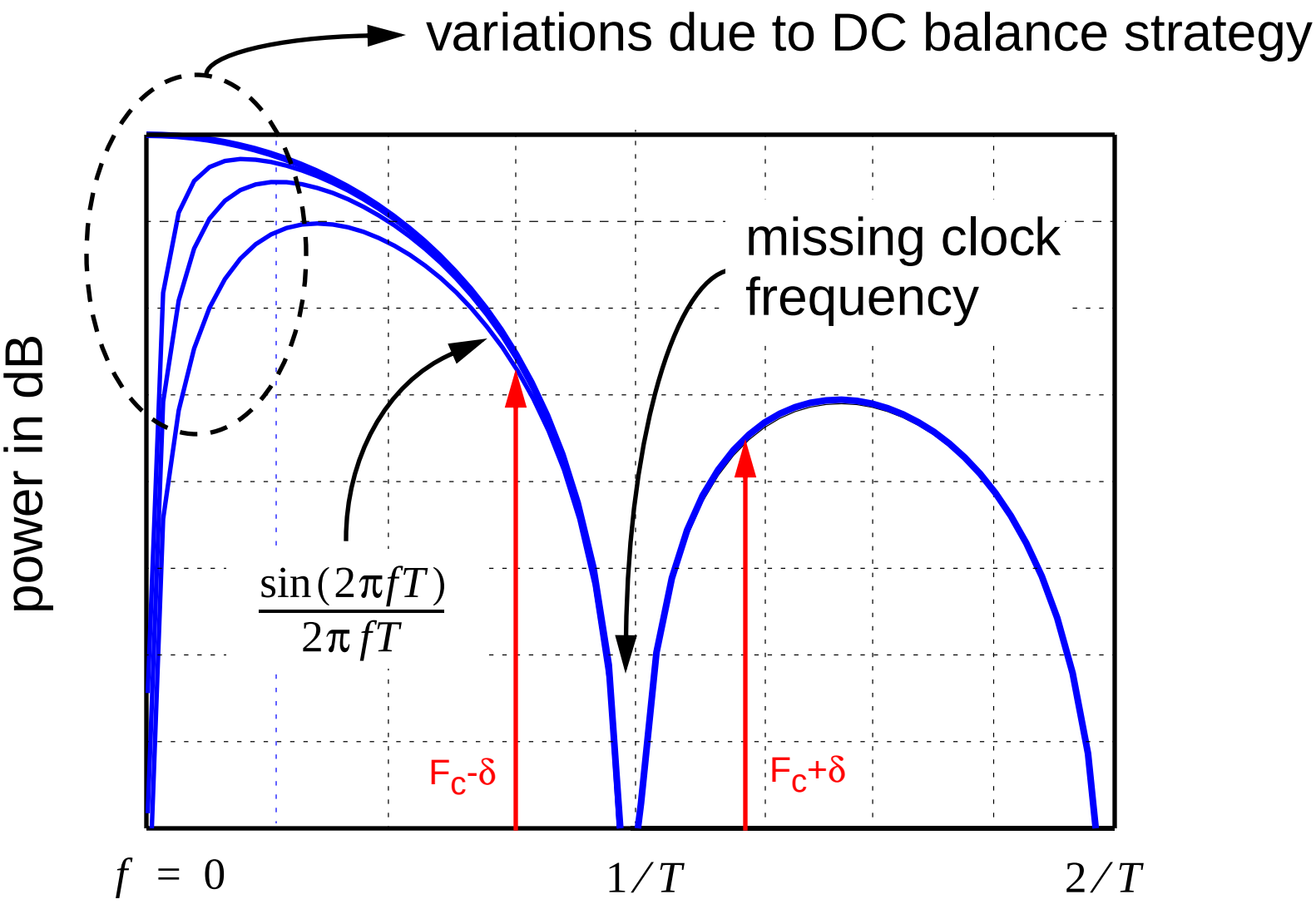


RZ = “return to zero” data

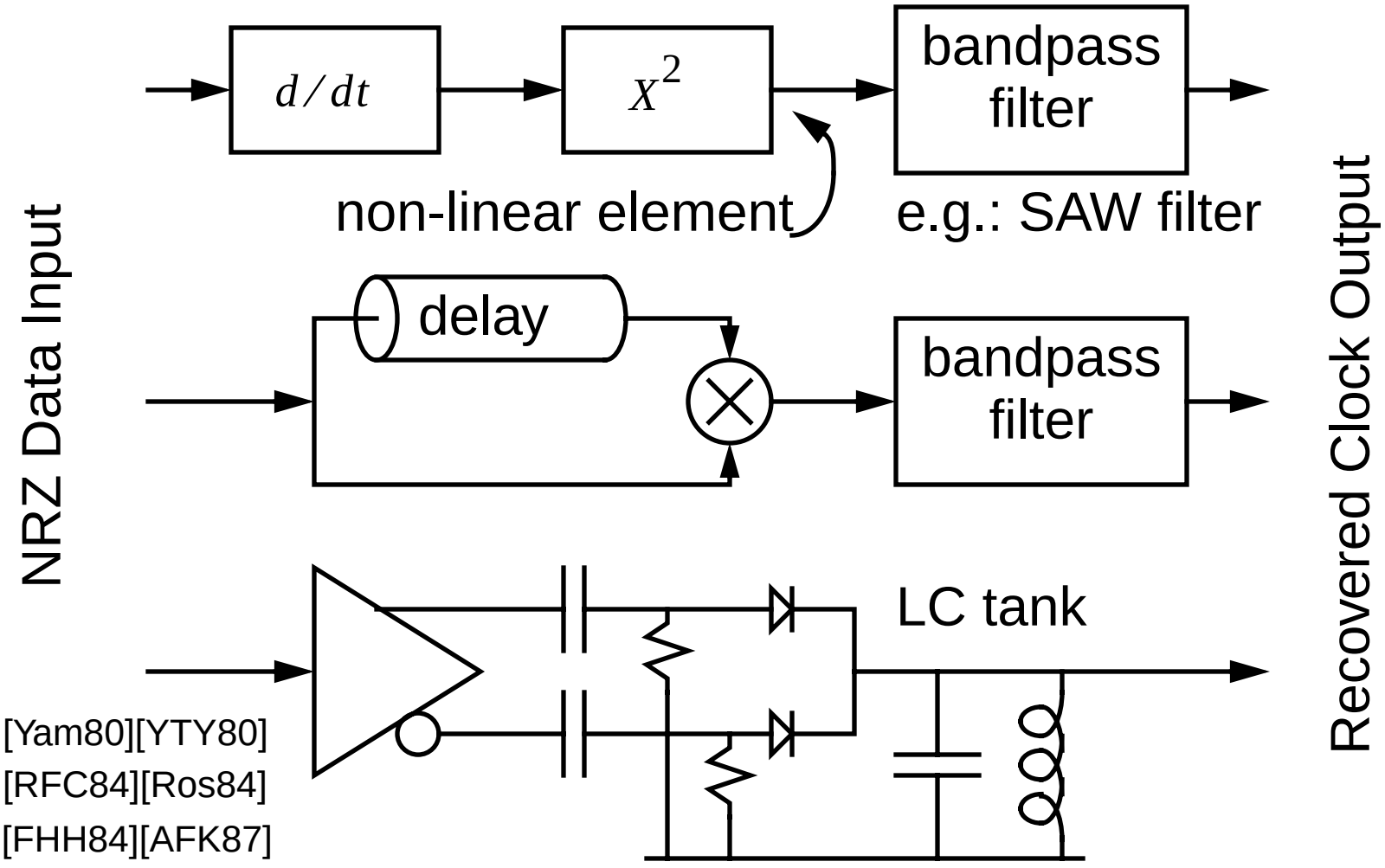


NRZ signalling is almost universally used.

Spectrum of NRZ data

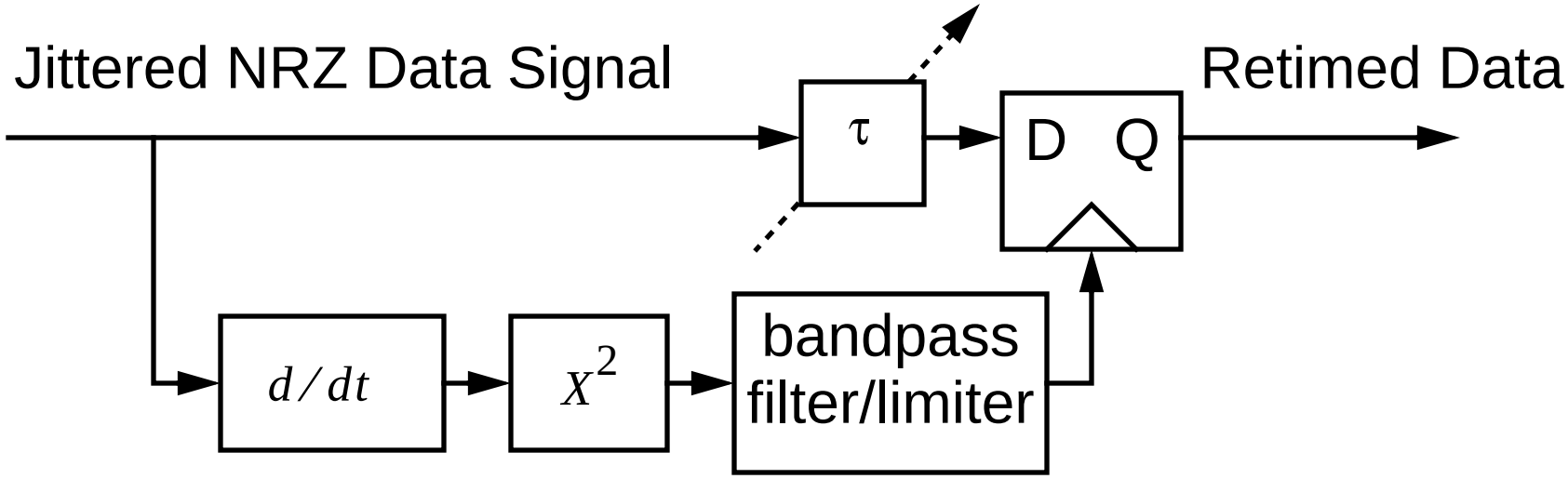


Filter Method Examples



(this last circuit can be thought of as an NRZ-RZ converter)

Summary of Filter Method



Pro:

Very simple to implement

Can be built with microwave “tinkertoys” using coax to very high frequencies

Con:

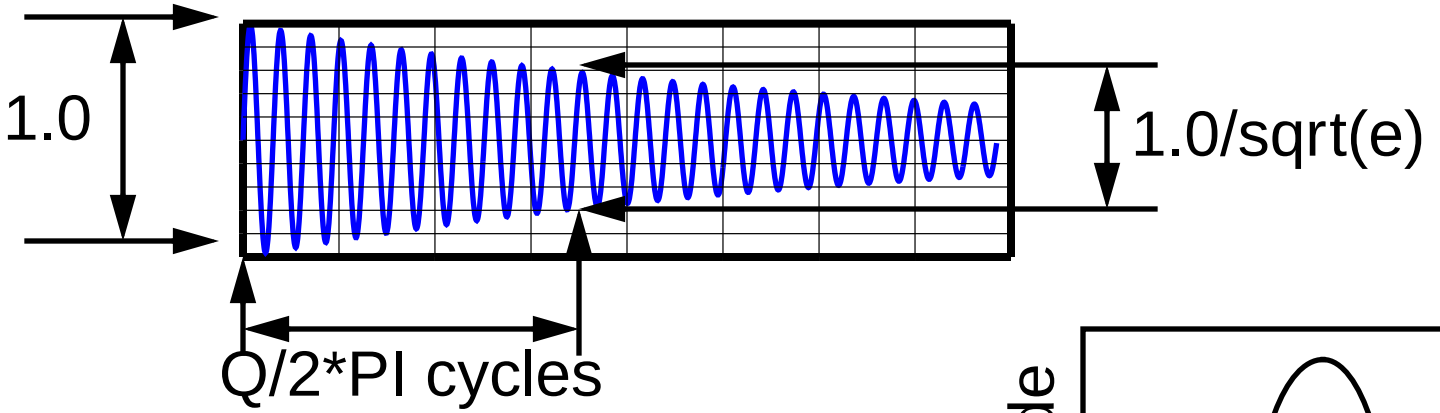
Temperature and frequency variation of filter group delay makes sampling time difficult to control

Narrow pulses imply high f_T

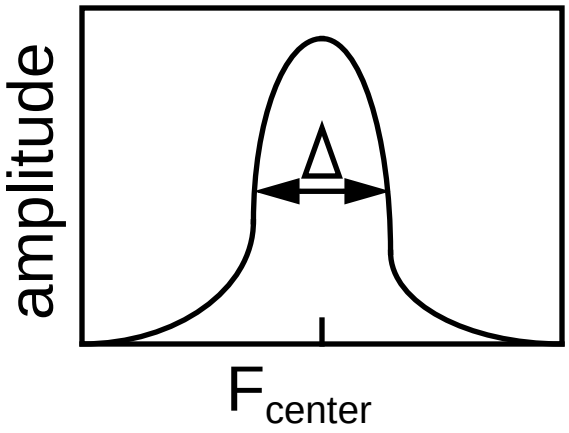
Hi-Q filter difficult to integrate

Q-Factor in resonant circuits

Voltage envelope of ringing circuit falls to 1/sqrt(e) in Q radians.

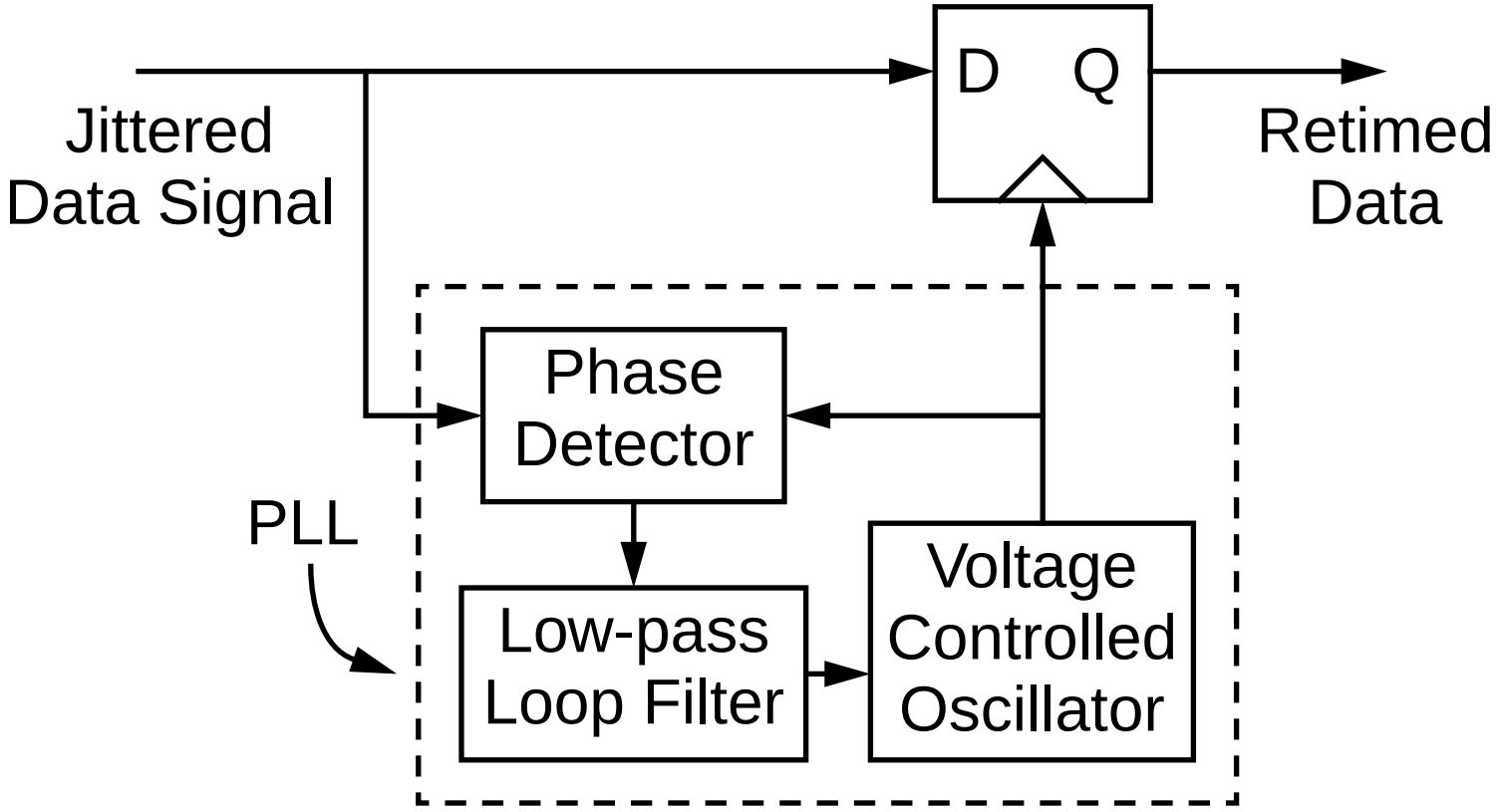


Q also equals the center frequency of a filter divided by the full-width of the resonance measured at the half power points: $F_{center}/\ \Delta$



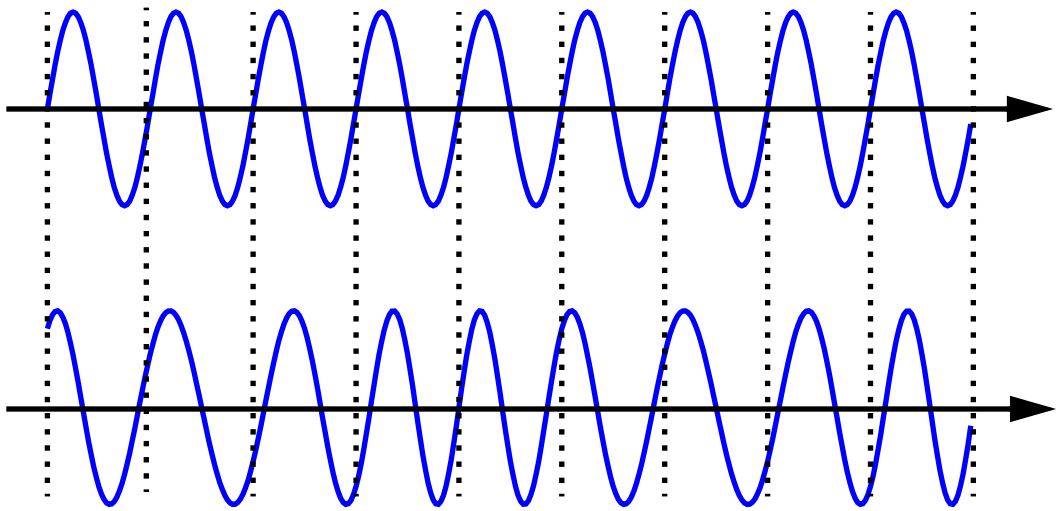
High-Q filter can be emulated by PLL with low loop B.W.

Data recovery with simple PLL



Everything in the simple PLL is easily integrable. The remaining problem is to match the recovered clock phase to the middle of the data eye. This can be difficult to achieve over all process variation at very high datarate/f_t ratios.

Analytic Treatment of Jitter

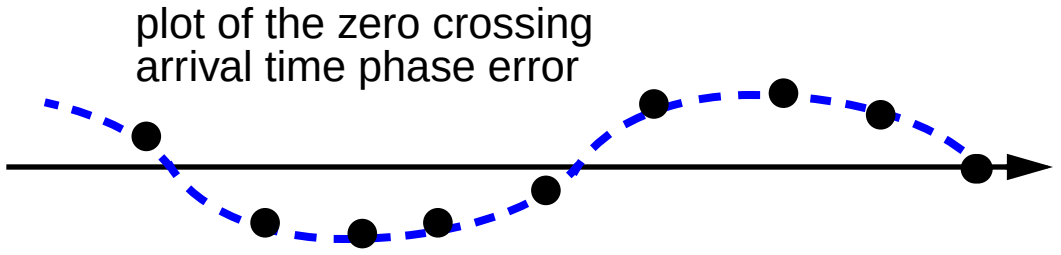


Perfect Clock:

$$x(t) = A\cos\omega_c t$$

Jittered Clock:

$$x(t) = A\cos[\omega_c t + \phi(t)]$$

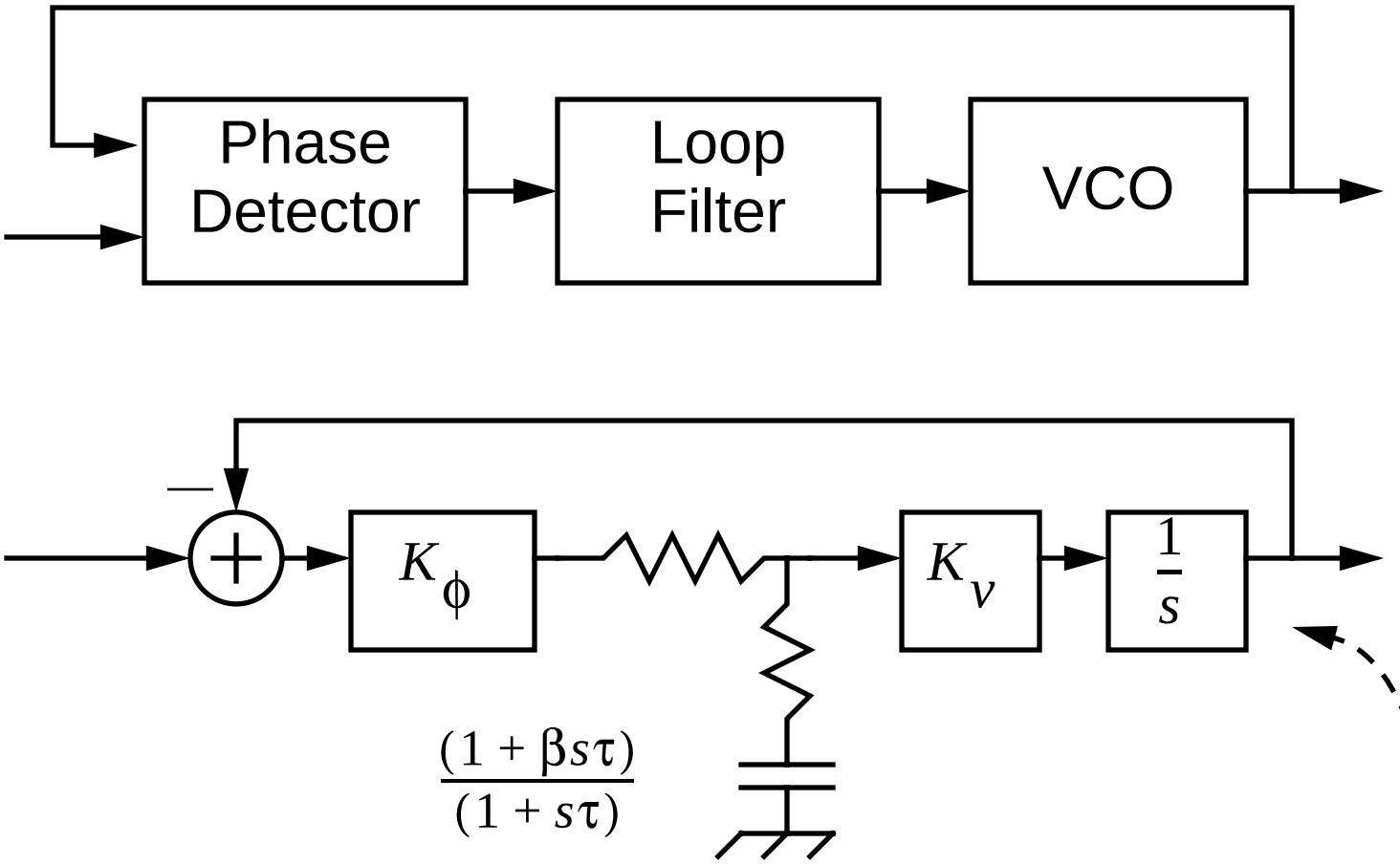


Jitter Signal:

$$x(t) = \phi(t)$$

Practically, $\phi(t)$ is only measured at zero crossings, but is treated as a continuous time signal.

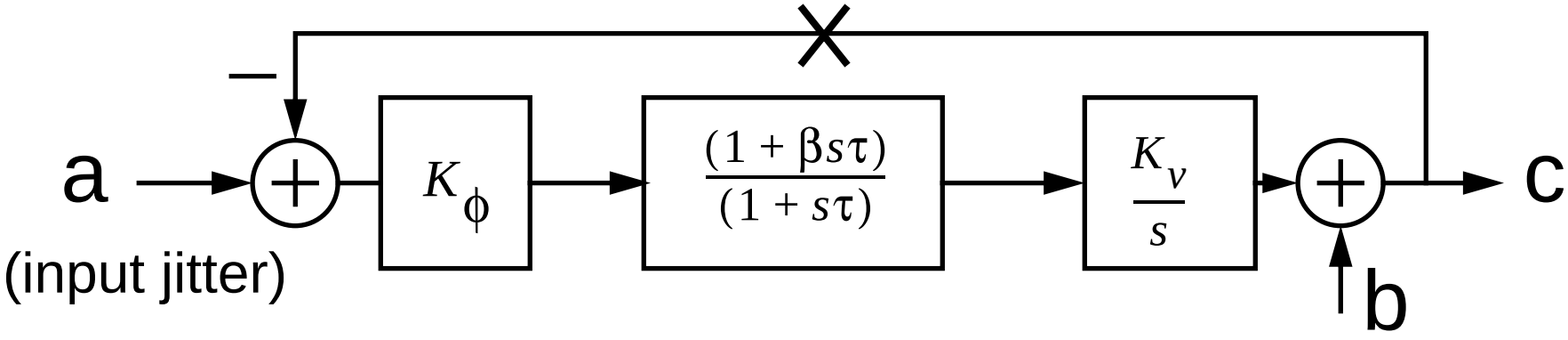
Model of linear phase-locked loop

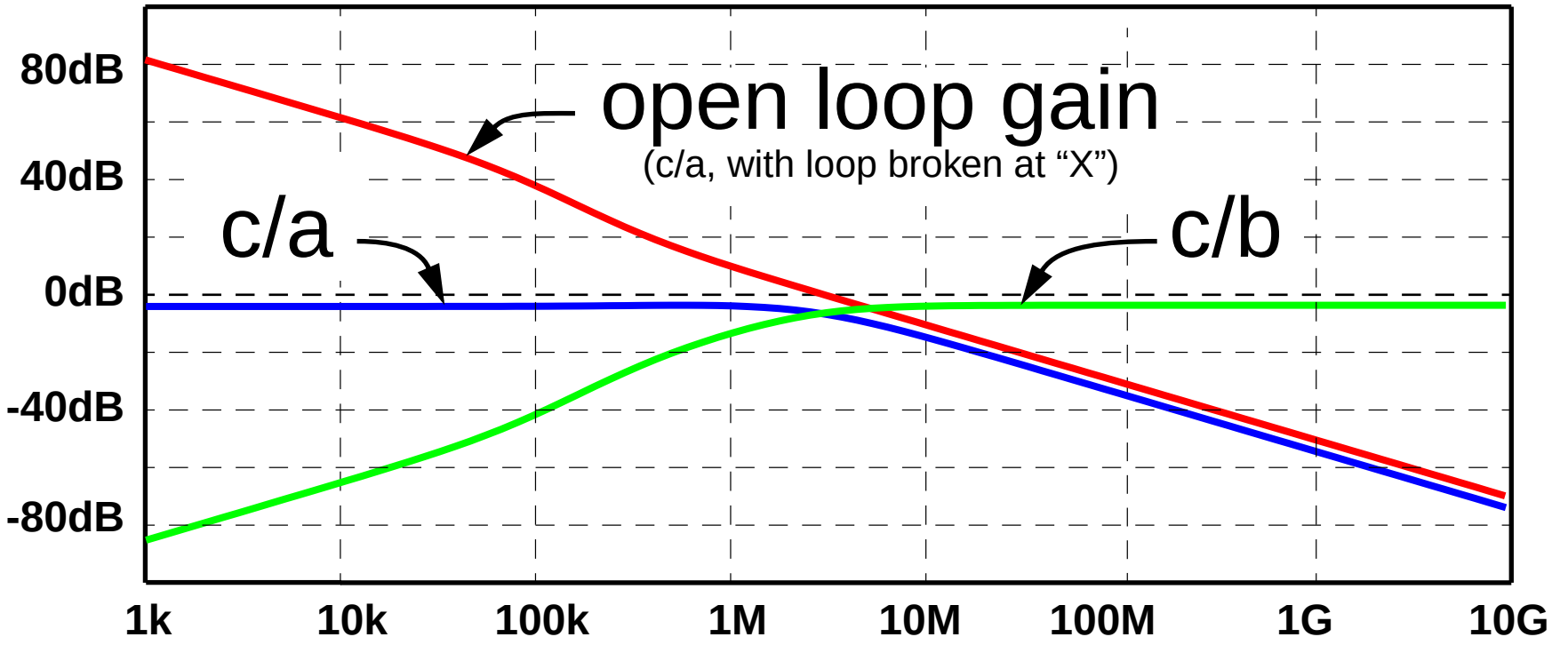


Warning: Extra integration in VCO complicates the design!

See Floyd M. Gardner, “Phaselock Techniques”, John Wiley and Sons, for good introduction to PLL theory

Linear loop frequency response

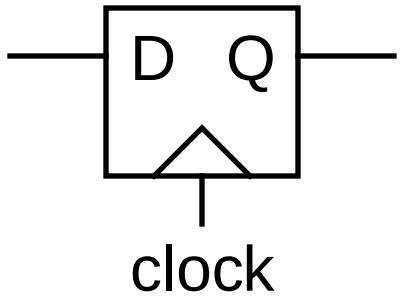




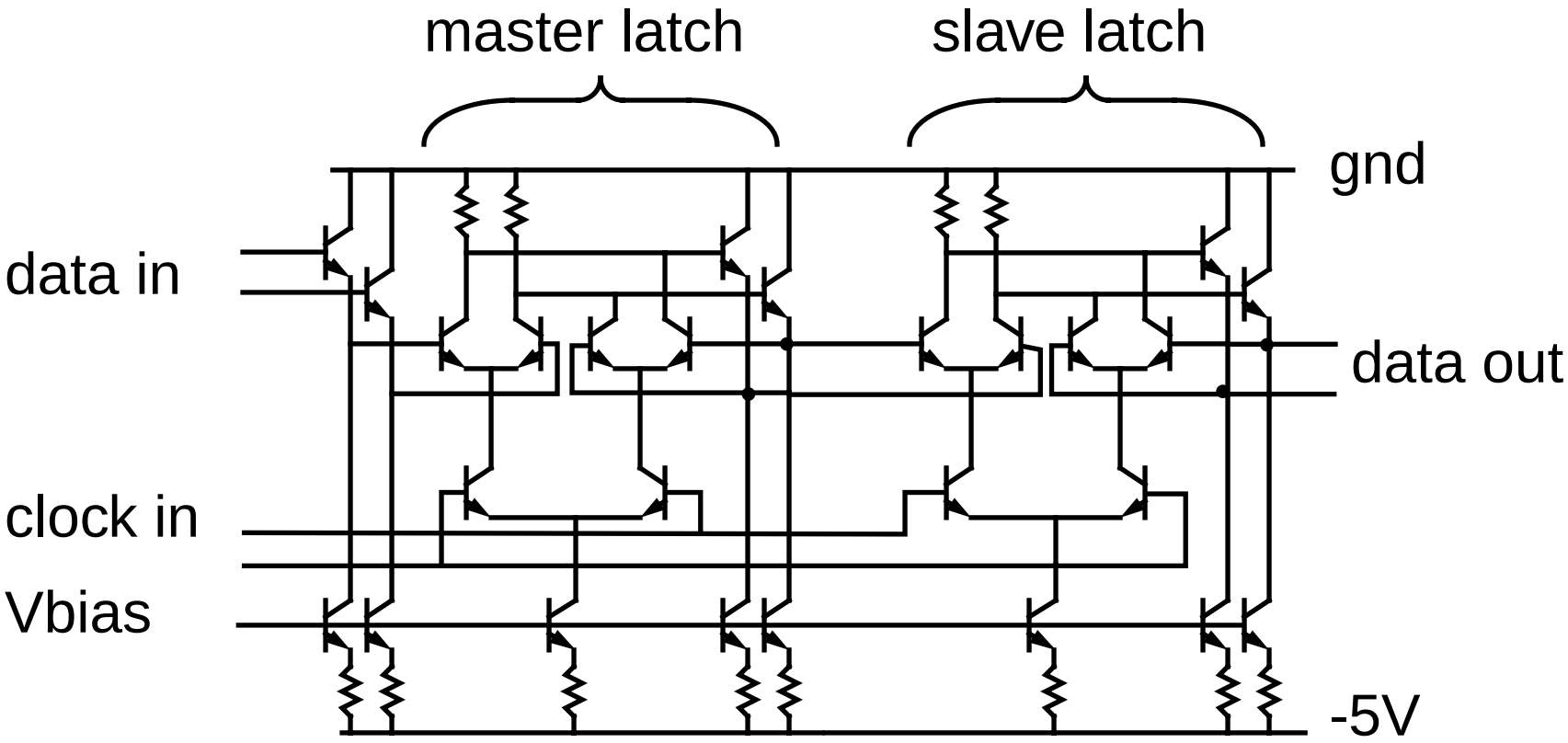
Decision Circuit

- Quantizes amplitude at precise sample instant and typically uses positive feedback to resolve small input signals
- A common choice in bipolar processes is a master/slave D-flip-flop carefully optimized for input sensitivity and clock phase margin
- To avoid hysteresis in CMOS processes, it is common to use a sense amp which is reset prior to each data sample

simplified schematic symbol:



Example Bipolar Decision Circuit



- many clever optimizations are possible

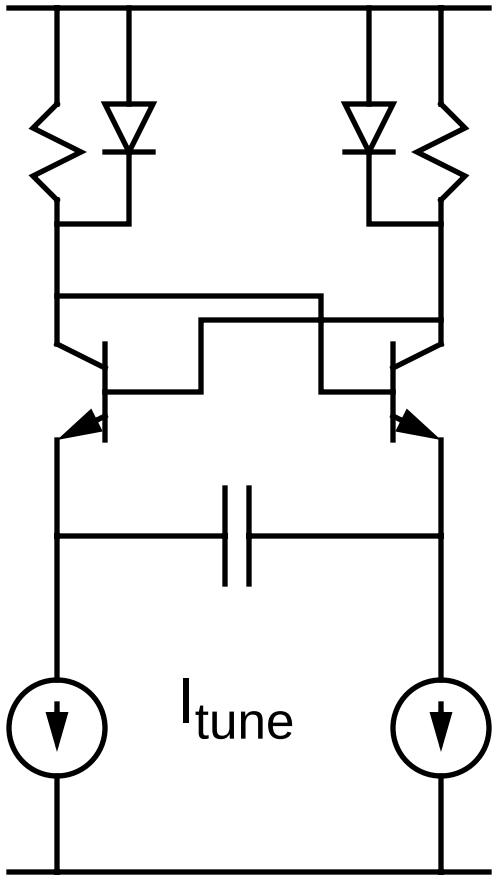
[OhT83][Con84][Lai90][Run91][Hau91]

VCO alternatives

	LC Oscillator	**Multivibrator**	**Ring Oscillator**
Speed	Technology Dependent 1-10's of GHz		
Phase Noise	Good	Poor	
Integration	Poor (L, Varactor)	Excellent	
Tunability	Narrow/Slow	Wide/Fast	
Stability	Good	Poor (needs acquisition aid)	
Other			Multi-Phase Clocks

- [Cor79, Ena87, Wal89, DeV91, Lam93, WKG94]

Multivibrator VCO



Capacitor is alternately charged and discharged by constant current

Tuned by varying I_{tune} in current source

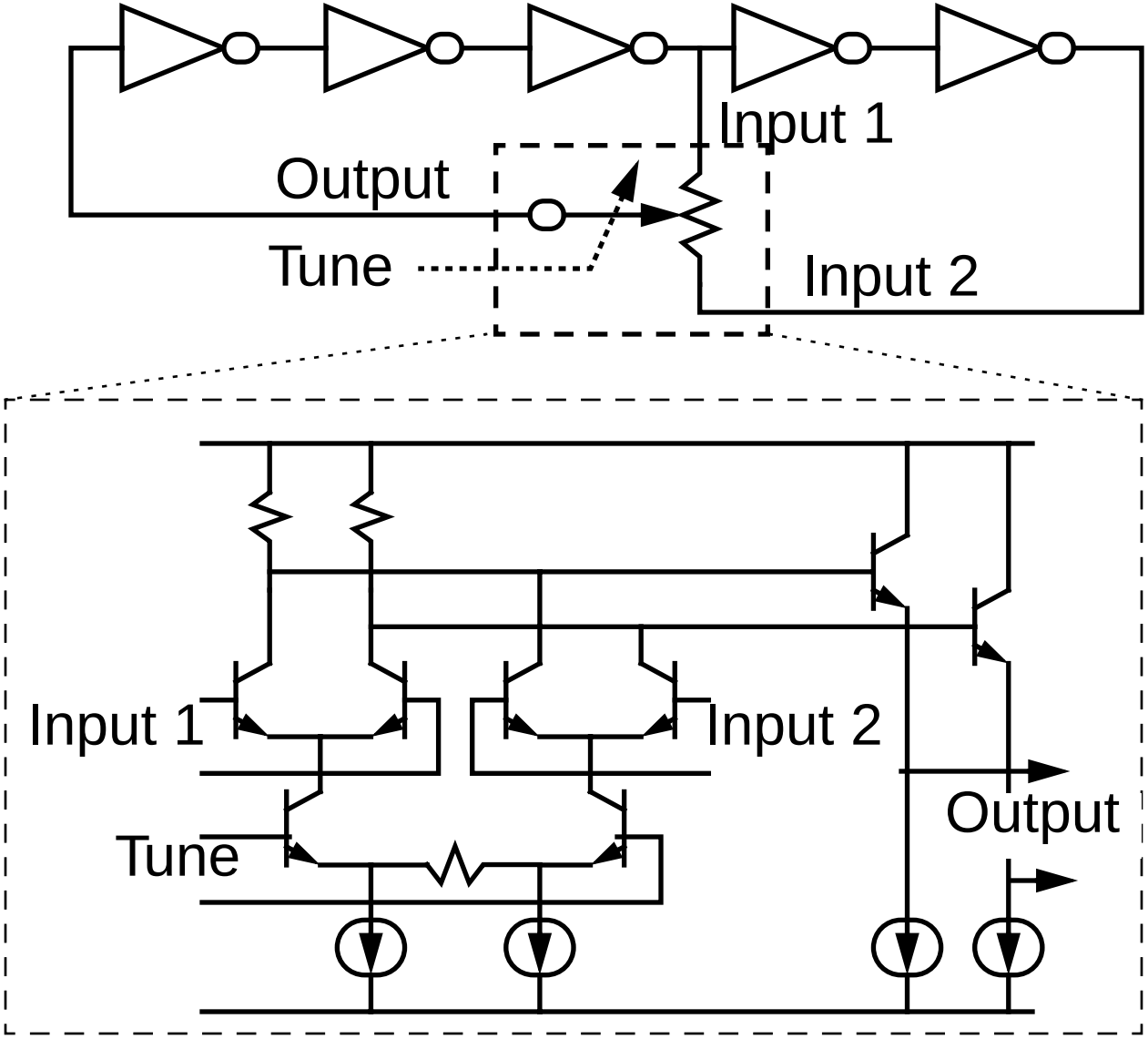
Diode clamps keep output voltage constant independent of frequency

Relies on non-linear switching for oscillation behavior, and so is limited to moderate frequencies.

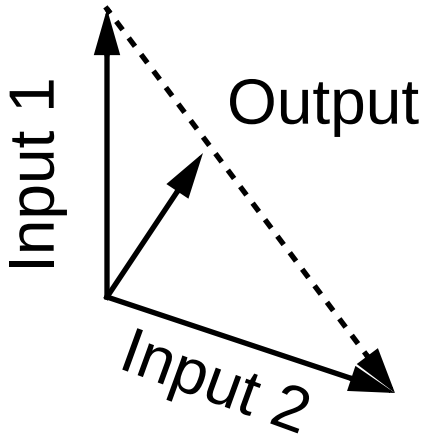
Frequency = $\frac{I_{tune}}{4CV_{be}}$

After Alan B. Grebene, “Analog Integrated Circuit Design”, Van Nostrand Reinhold, 1972, pp 313-315

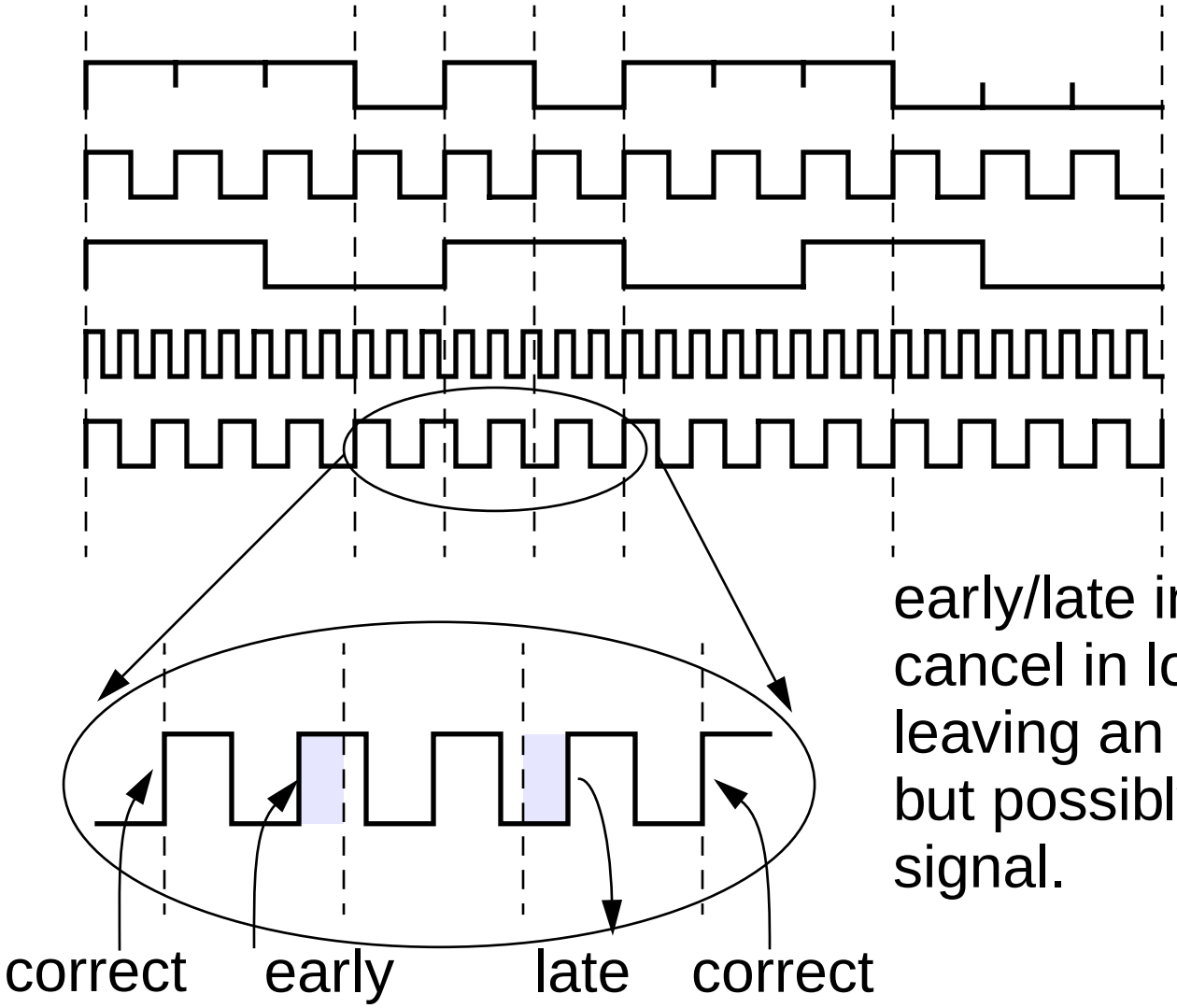
Example Ring Oscillator VCO



[SyA86]
[EnA87]
[Wal89]



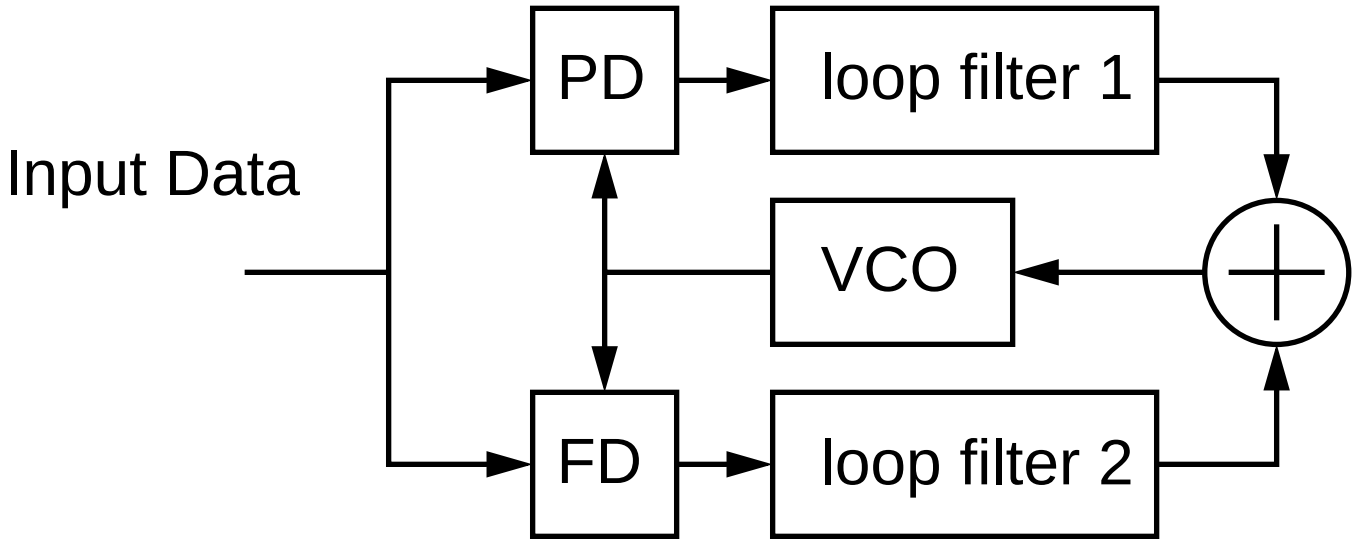
False or Harmonic Locking to Data



early/late indications cancel in loop filter, leaving an attenuated, but possibly stable lock signal.

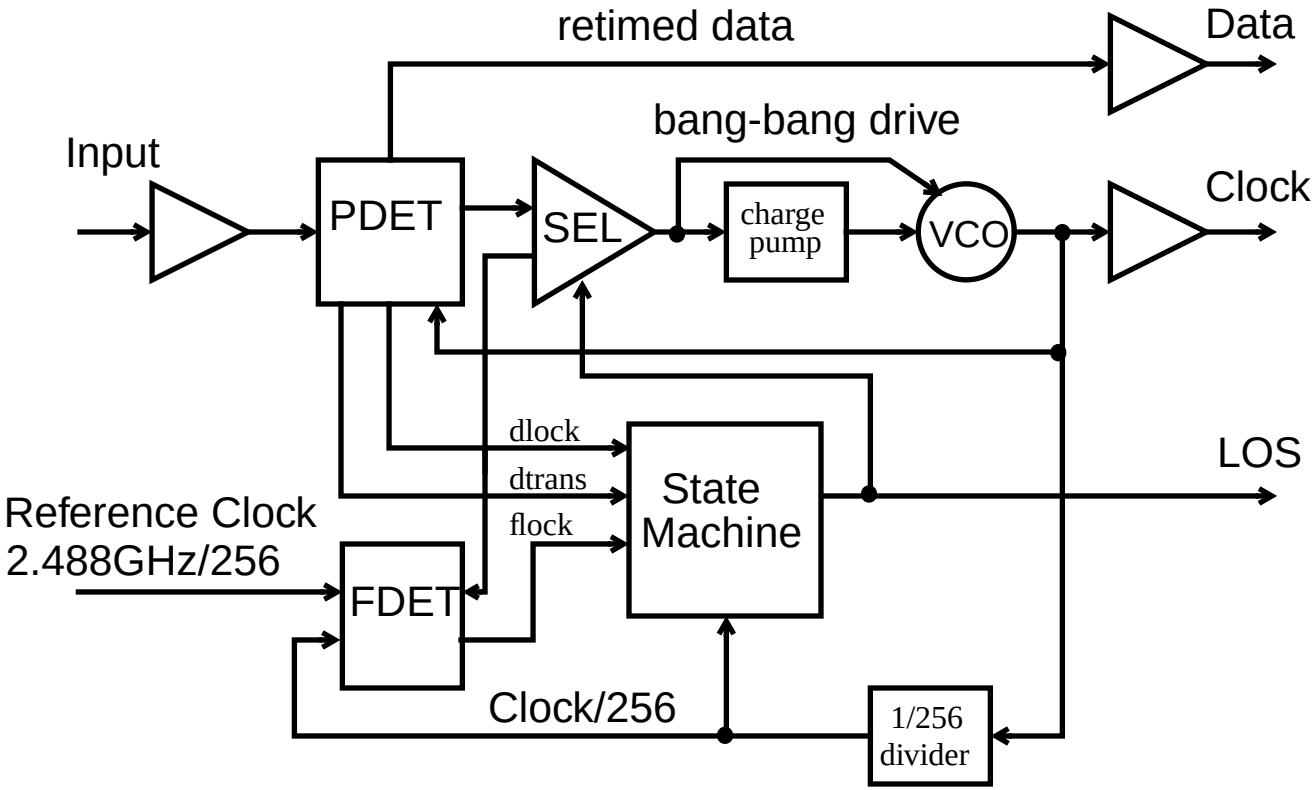
Aided Acquistion

- Tricky task due to Nyquist sampling constraints caused by stuttering data transitions



- Still subject to false lock if VCO range is too wide

Training Loops

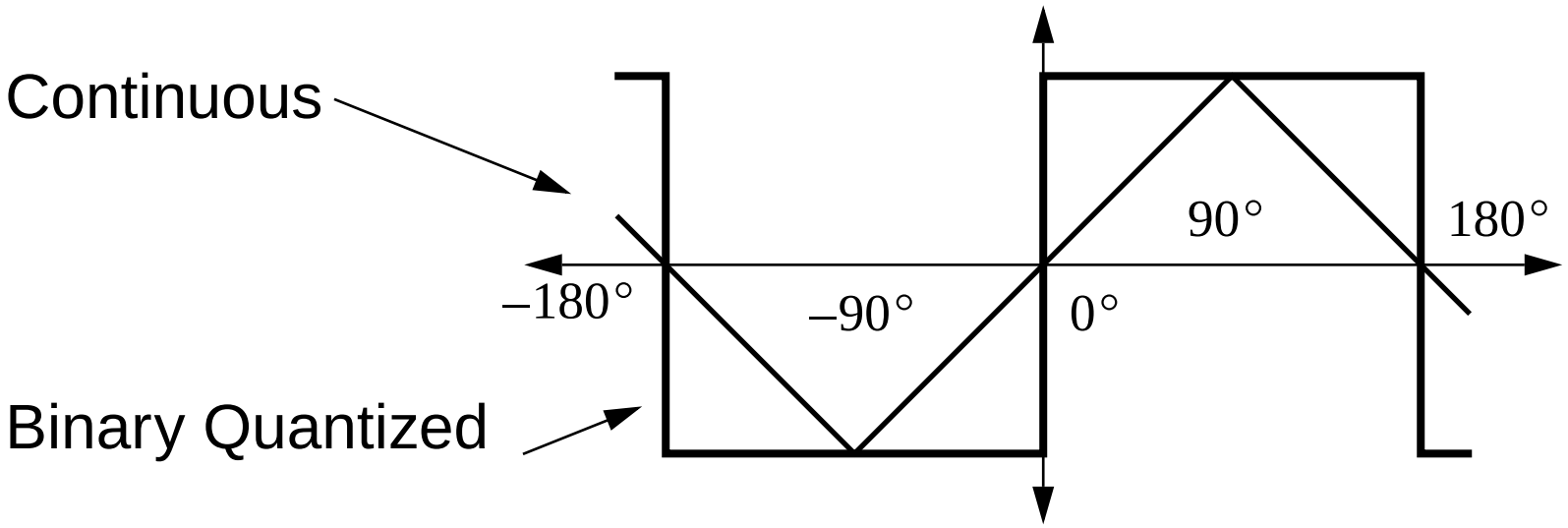


[WSY97]

An increasingly common technique is to provide a reference clock to the CDR circuit. This allows the VCO process-variation to be dynamically trimmed out, avoiding false locking problems.

Phase Detectors

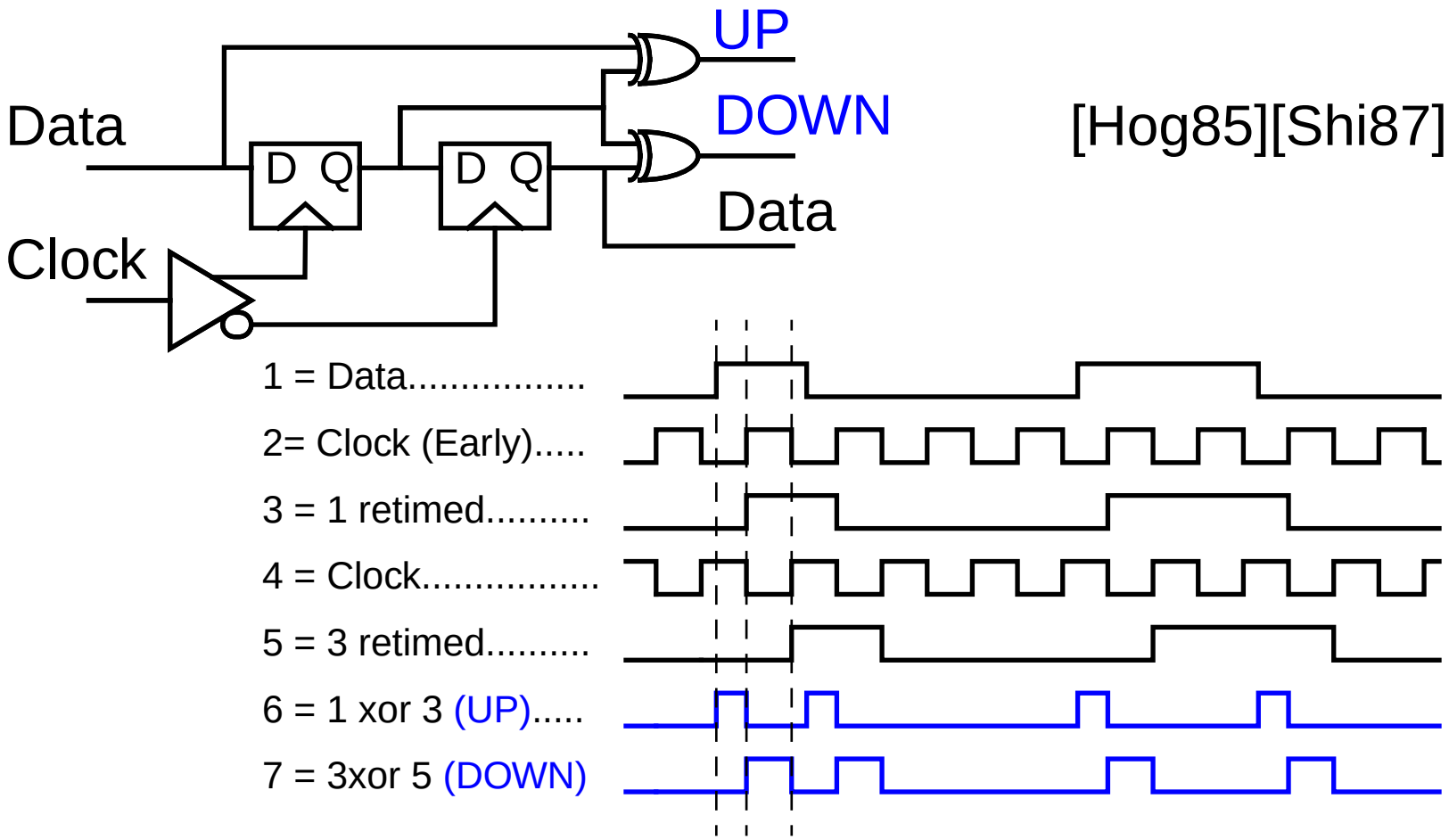
- Phase detectors generate a DC component proportional to deviation of the sampling point from center of bit-cell
- Phase detectors are:



- Binary quantized phase detectors are also called “Bang-bang”, or “early-late” phase detectors

After [Hor92].

“Self-Correcting Phase Detector”

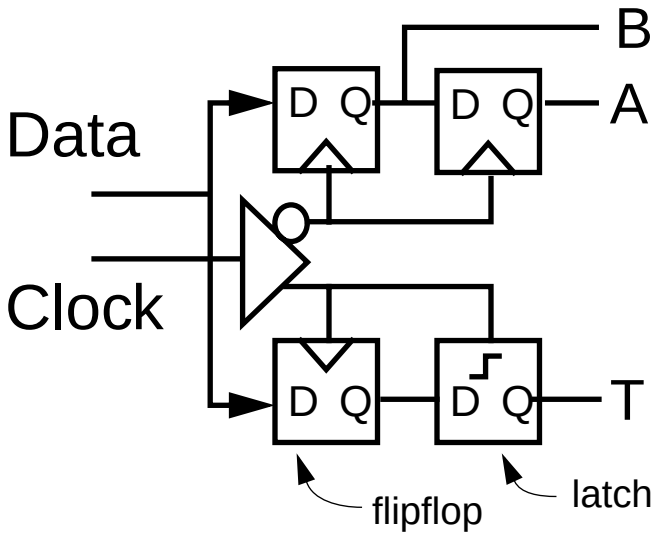


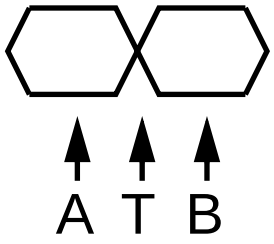
[Hog85][Shi87]

The “Hogge” detector is typical of linear phase detectors. It operates by creating pulses whose widths are equal to the phase error of the incoming data. These pulses may be difficult to produce at high speeds.

Early-Late Phase Detector

- NRZ data is sampled at each bit cell and near the transitions of each bit cell
- Transition sample polarity is compared with preceeding and following bits to deduce the phase error.
- Output is binary quantized, early-late phase indications, or ternary quantized if a hold-state is implemented.

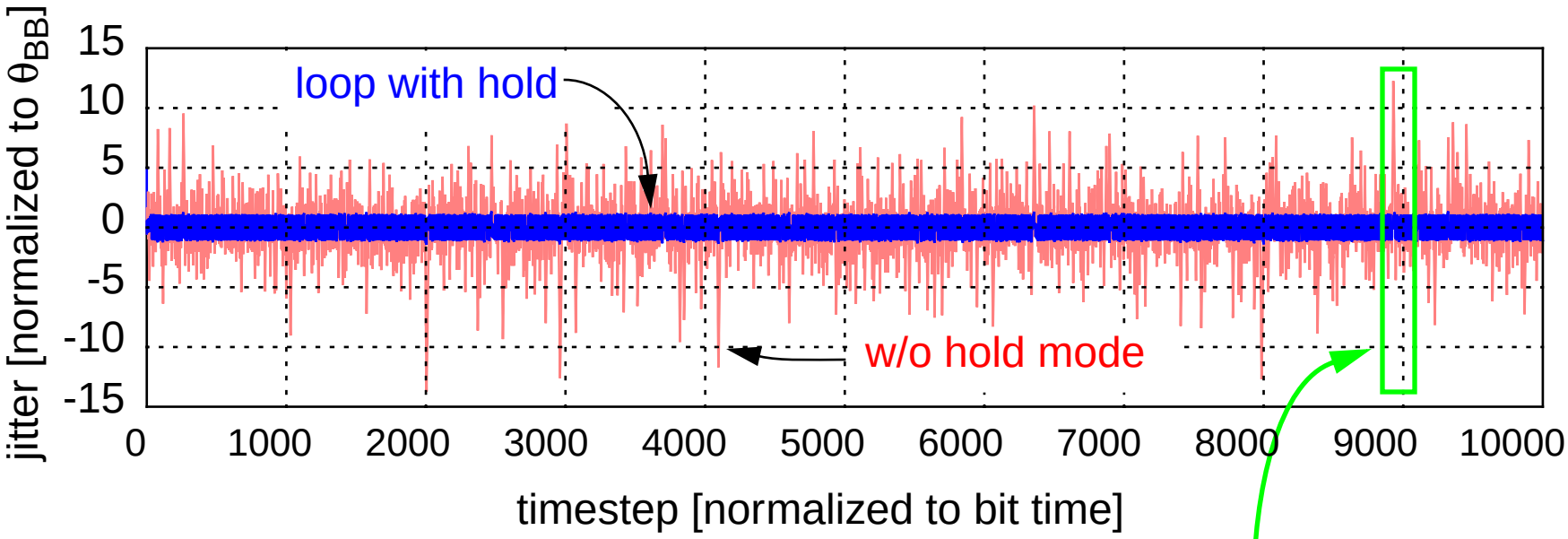




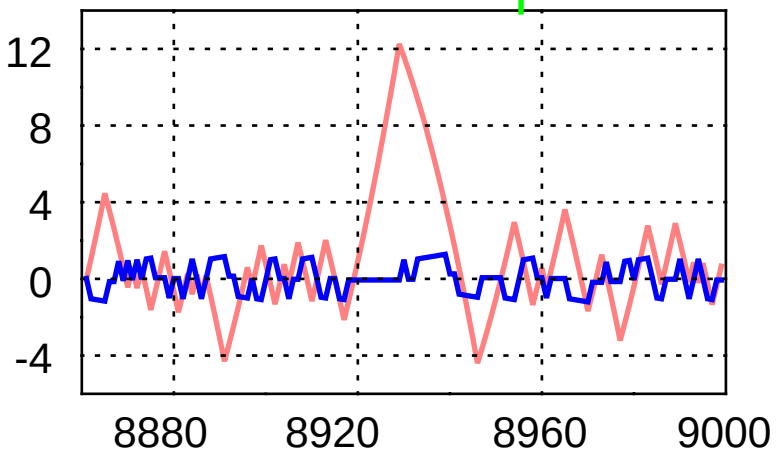
[Ale75][WHY91]
[LaW91][ReG73]

A	T	B	Output
0	0	0	hold
0	0	1	vco fast
0	1	0	?
0	1	1	vco slow
1	0	0	vco slow
1	0	1	?
1	1	0	vco fast
1	1	1	hold

BB/charge-pump w/wo hold state

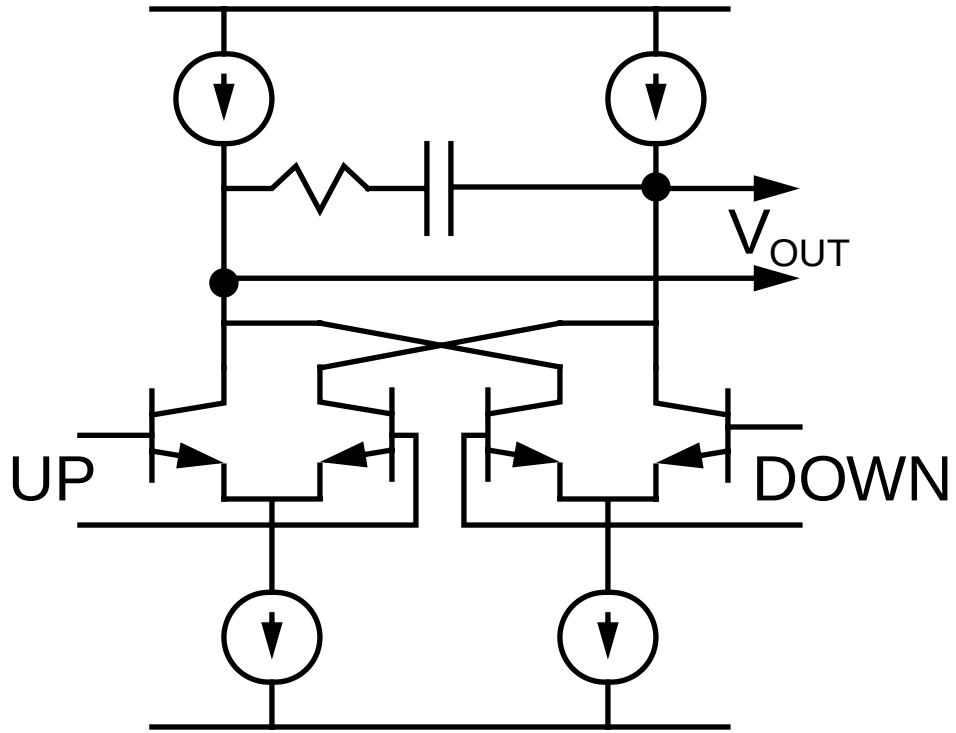


- hold-mode maintains VCO frequency when transitions are absent in the data.
- loop w/o hold has peak jitter *run-length* times worse than loop w/hold



(simulated with ξ=100, $p_{transition}$ = 50%)

Loop Filters



[Den88] [Dev91]
[LaW91] [WuW92]

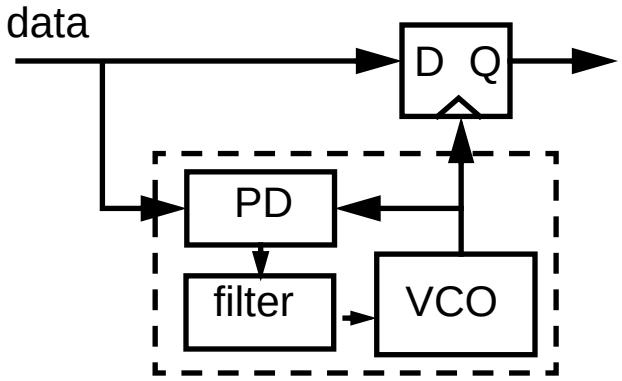
UP	DOWN	V_{OUT}
0	0	hold
0	1	ramp DOWN
1	0	ramp UP
1	1	hold

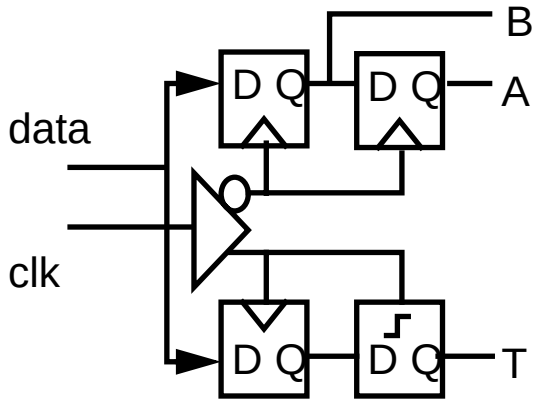
- should have provision for holding value constant under long run-length conditions
- may be analog (integrator) or digital (up-down counter) - but *watch out for metastability*!

Bang-bang PLL Theory

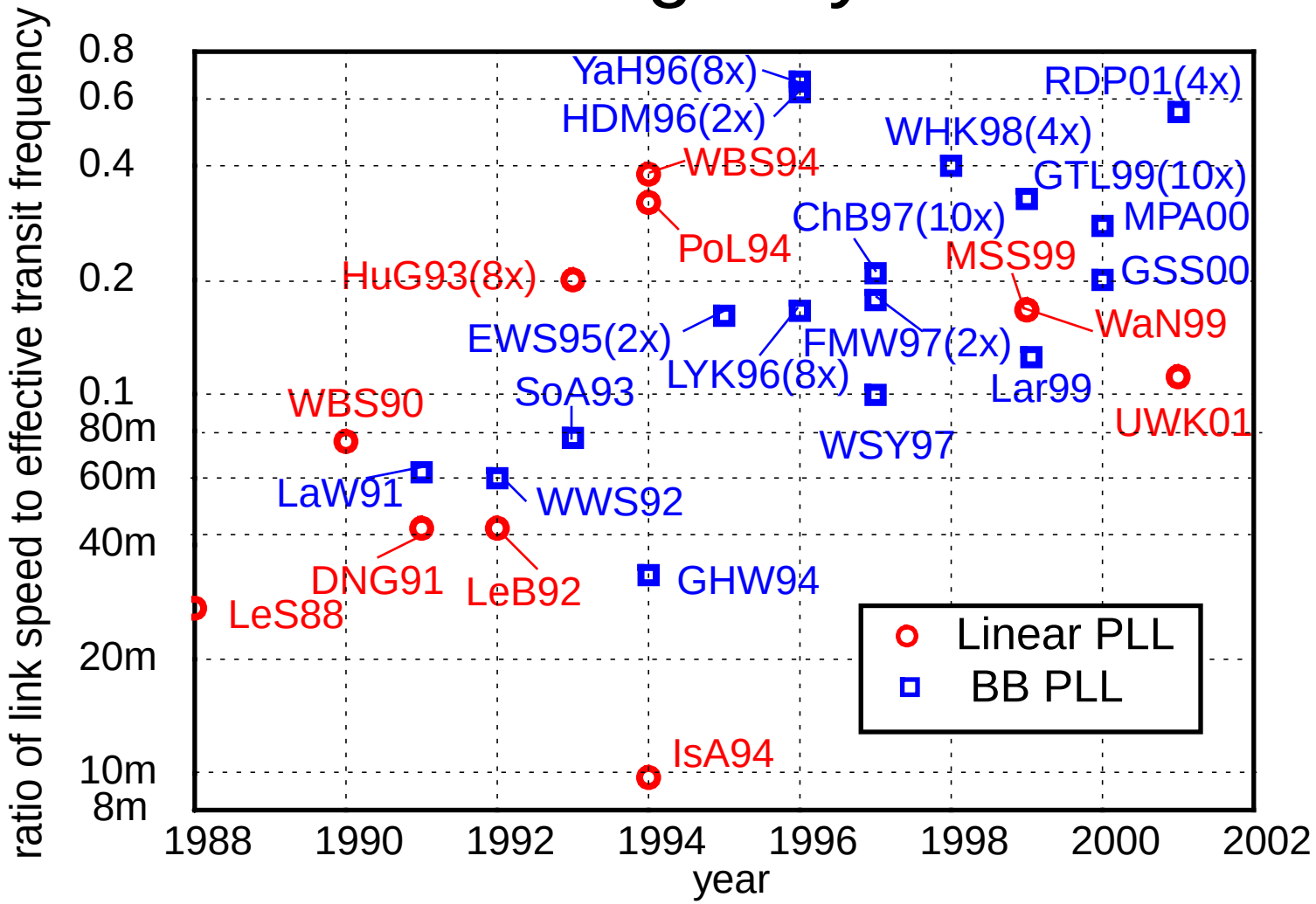
Why bother with a BB loop?

- it may be difficult to maintain optimum sampling point with traditional PD/PLL or with filter method over process, temperature and supply variation
- Narrow pulses of linear PD's may not work well at extremely high bit rates
- for monolithic implementation, BB PD has excellent match between retiming latch and PD latch - allows for operation at highest latch toggle frequency



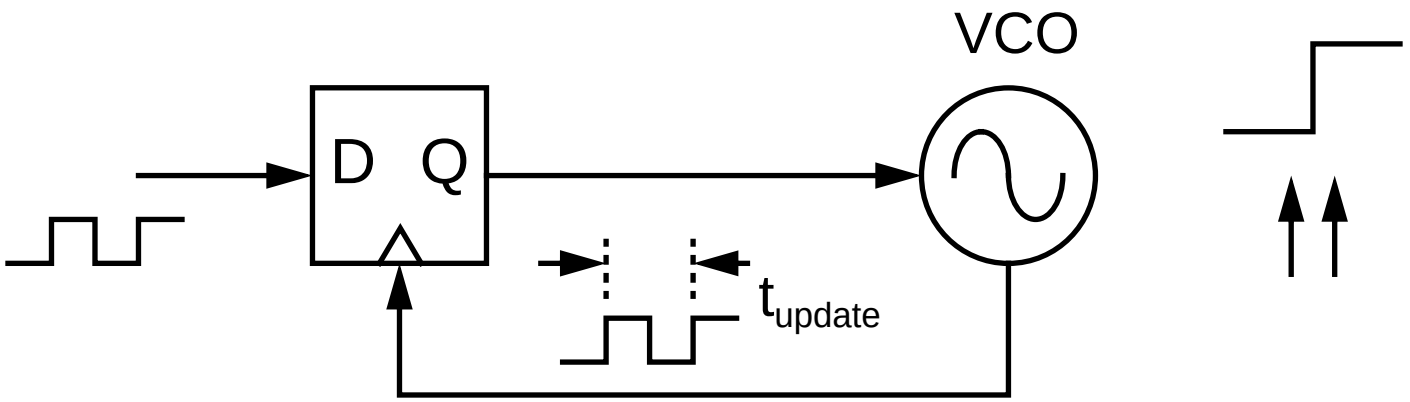


CDR PLL design style over time



BB PLLs have the advantage of precise sample point alignment based on layout symmetry. This makes BB PLLs predominate as designs push data rate towards the process transit frequency limit. (number of retiming phases shown in ()).

Simple First Order BB loop

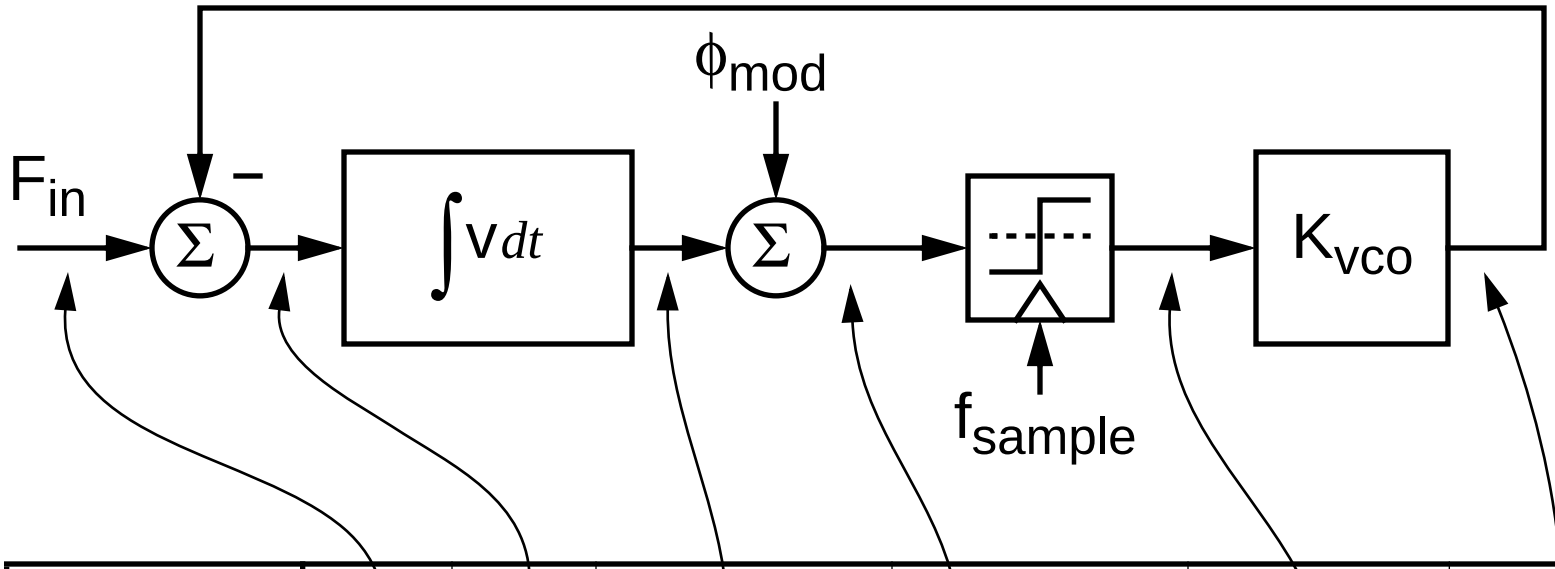


- VCO runs at two discrete frequencies: $f_{nom} \pm f_{bb}$.
- Phase error is evaluated at a discrete time interval t_{update}. In general, this can be approximated by the mean transition time of the data.
- A simple D-flip-flop serves as a bb-phase detector if locking to a clock rather than to a data signal.

Efficient Simulation Strategy

- Simulating the VCO *waveform* is unnecessary to accurately model ideal PLL behavior.
- Only frequency and phase is needed.
- Model all circuit time-varying state variables as voltages.
- Convert between frequency and phase variables with explicit integration block.

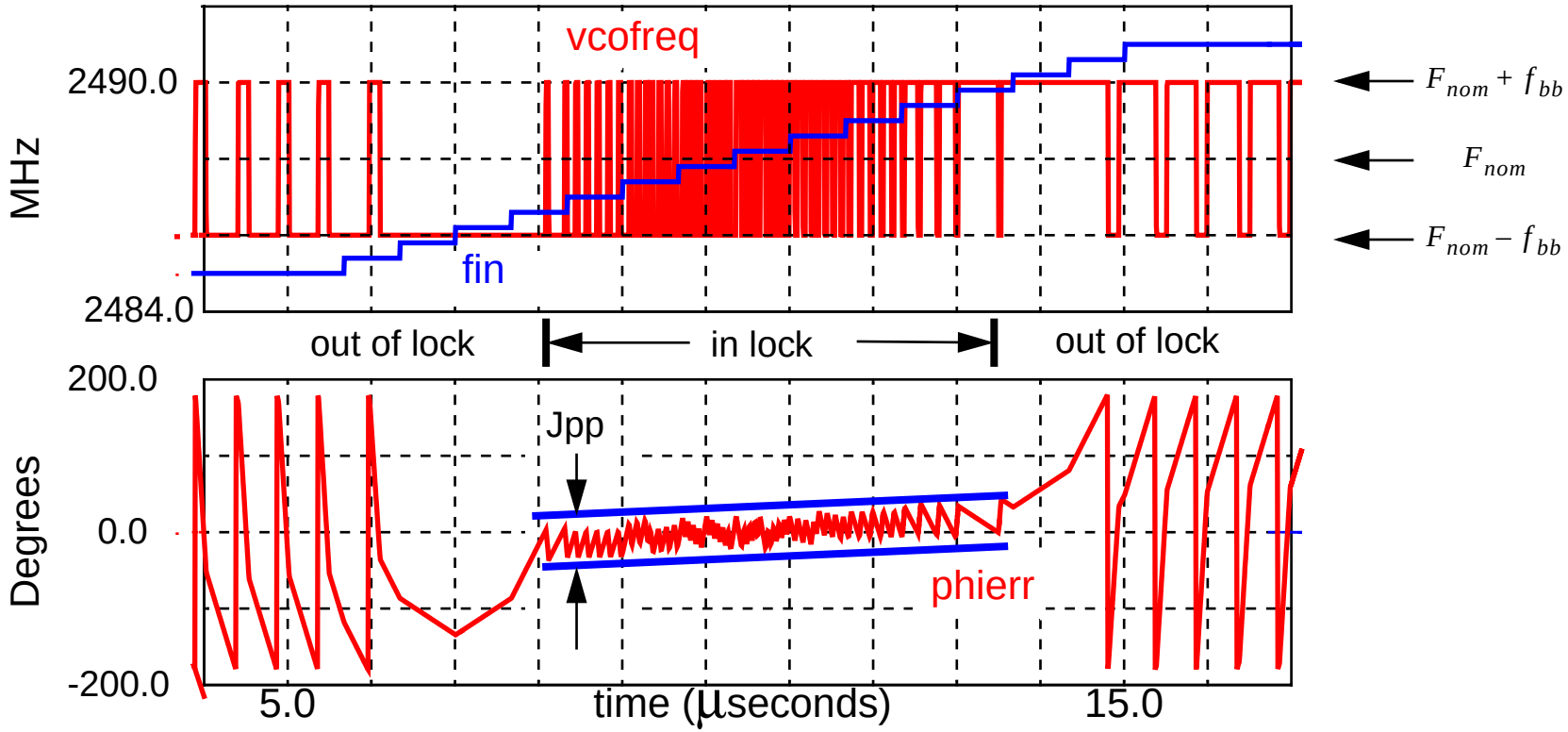
Model of First-order Loop



node:	F_{in}	ΔF	$\Delta\theta_1$	Θ_{error}	bbtune	F_{vco}
unit:	Hz	Hz	UI	UI	V	Hz

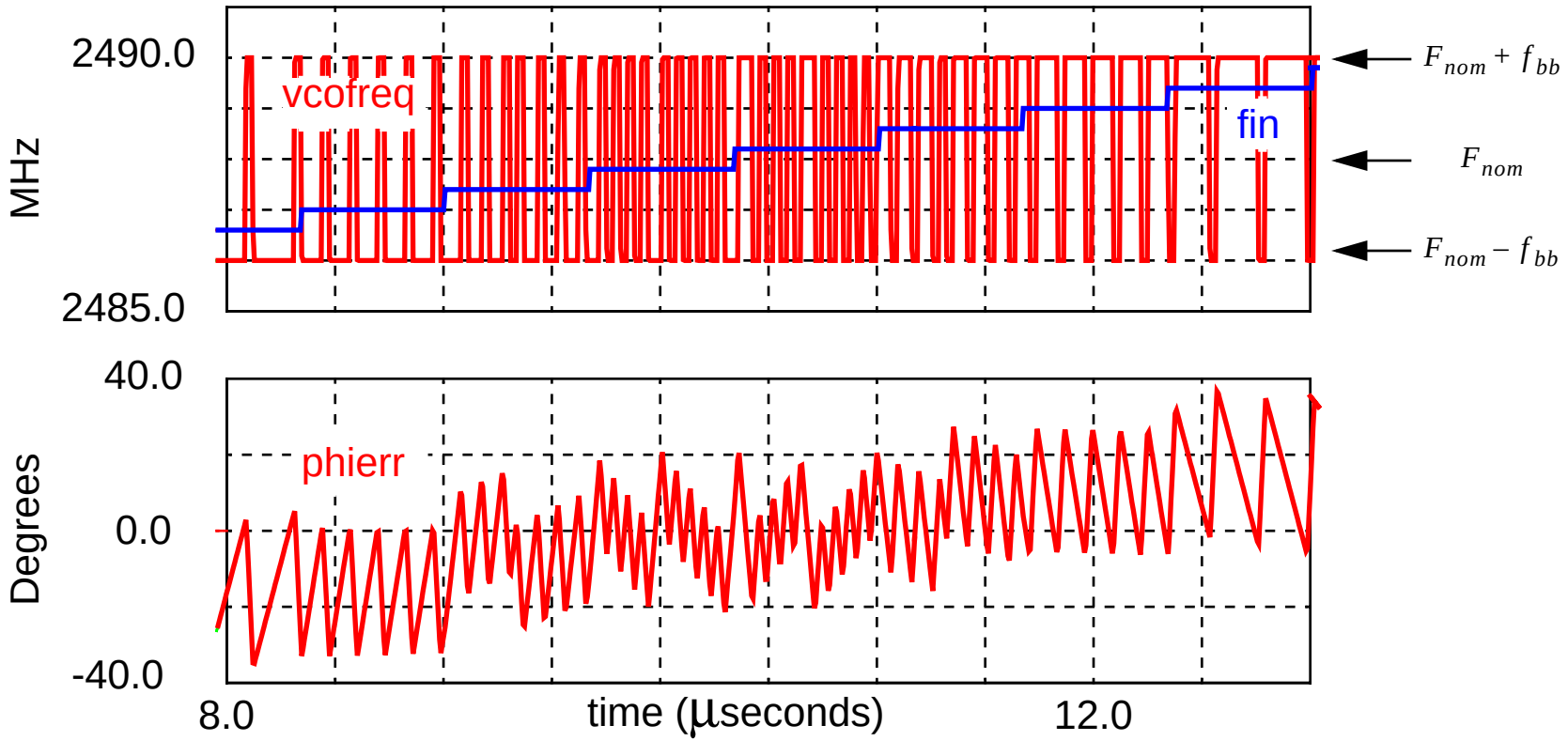
The tricky bit is to define the loop in terms of an input frequency rather than an input phase by pulling the VCO integral through the input summation. This allows easy simulation of both frequency and phase steps.

Lock Range for 1st-order loop



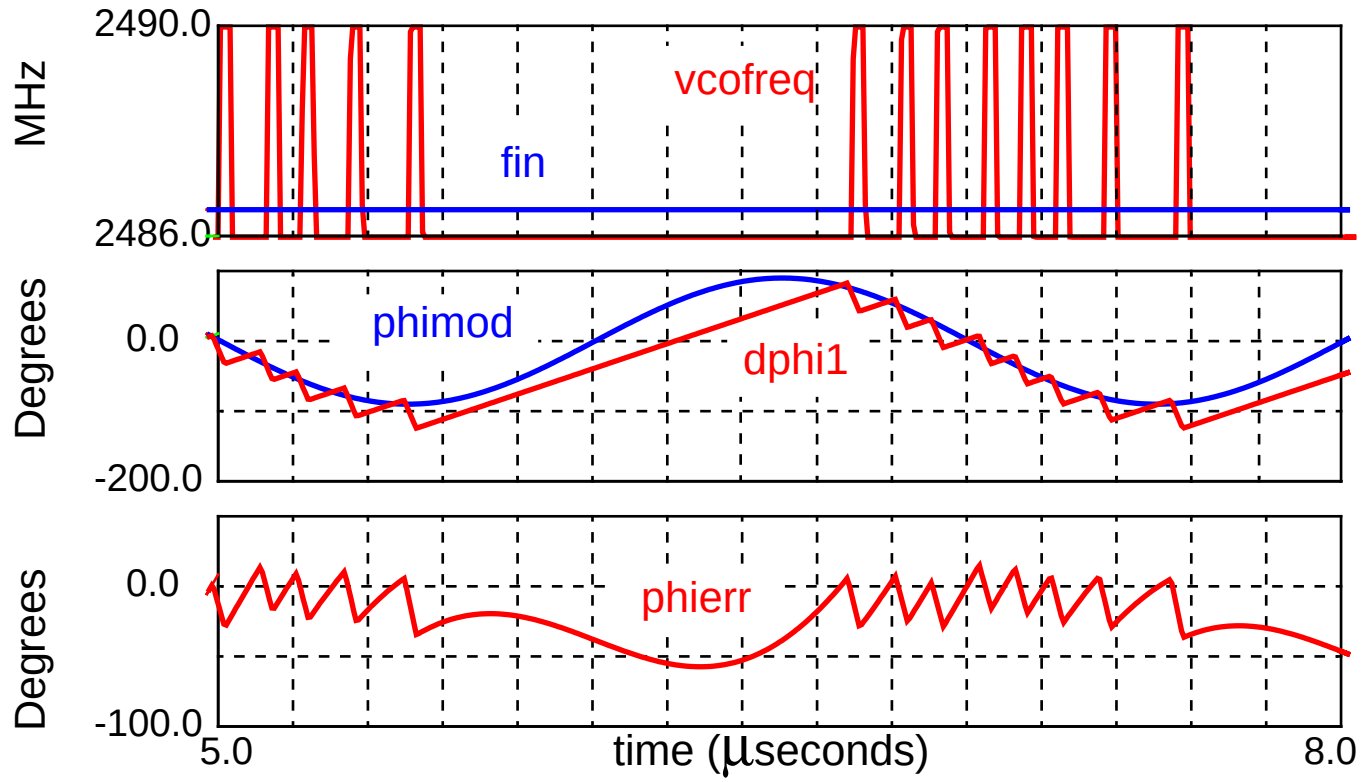
The loop is “locked” whenever the input frequency is bracketed by the two VCO frequencies. The rapid alternation between frequencies slightly too high and slightly too low create a hunting jitter (Jpp).

1st-order loop: locked region



The phase detector duty-cycle is proportional to the average frequency error.

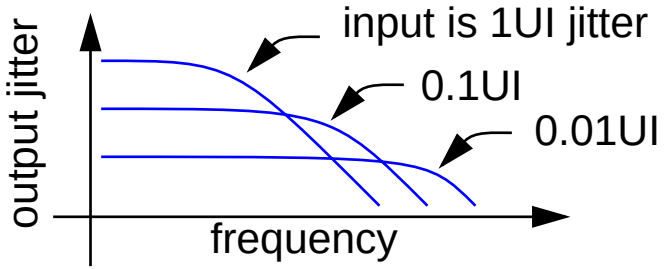
1st-order loop: slew-rate limiting



Although the average input frequency (fin) lies within the lock range of the loop, the added sinusoidal jitter (phimod) causes the instantaneous input frequency to exceed the VCO range. The loop phase (dphi1) stops toggling and goes into slew rate limiting, leading to a phase error (phierr).

Summary of 1st-order loop

- Lock range: $(f_{nom} - f_{bb}) < f_c < (f_{nom} + f_{bb})$.
- Jitter (pk/pk in UI): $J_{pp} = 2 \cdot t_{update} \cdot f_{bb}$.
- Bang-bang loop tracking is slew-rate limited. The effective loop bandwidth is amplitude dependent.



- The maximum amplitude of phase modulation at frequency f_{mod} before onset of slew-rate limiting: $A_{UI} = f_{bb} / f_{mod}$.

Summary of 1st-order loop, cont.

- If locked, then the duty cycle C, must result in the average loop frequency being equal to the input frequency f_c,

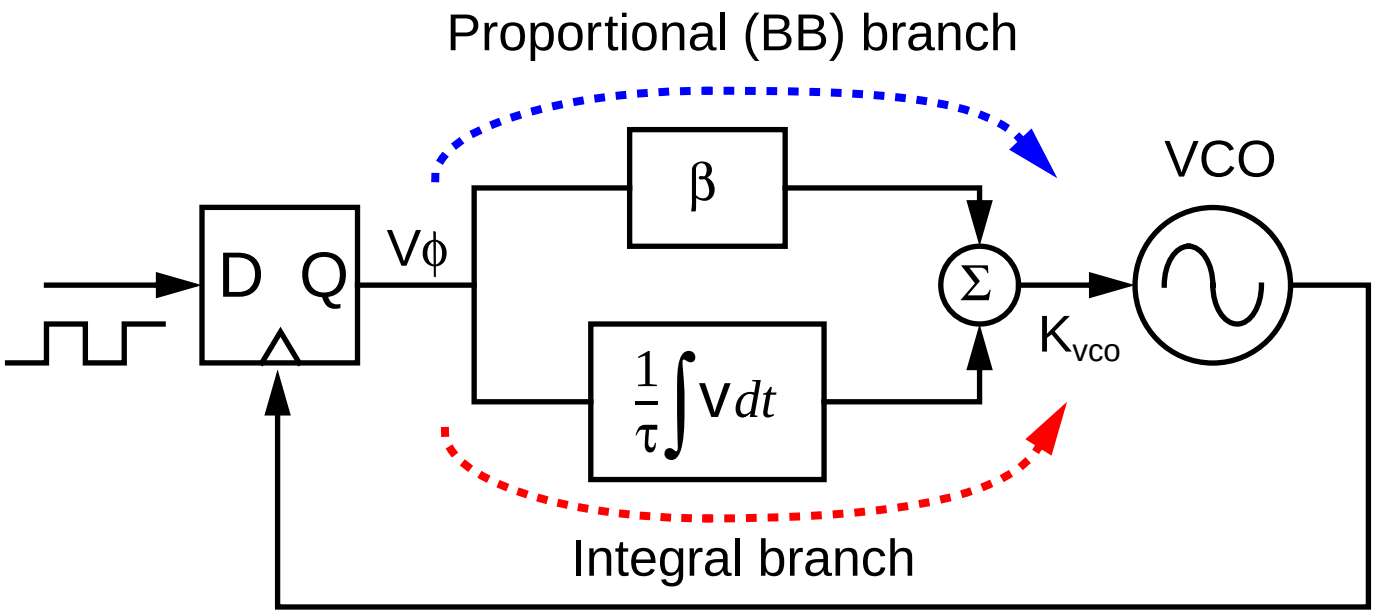
$$f_c = f_{nom} + \Delta f = C(f_{nom} + f_{bb}) + (1 - C)(f_{nom} - f_{bb})$$

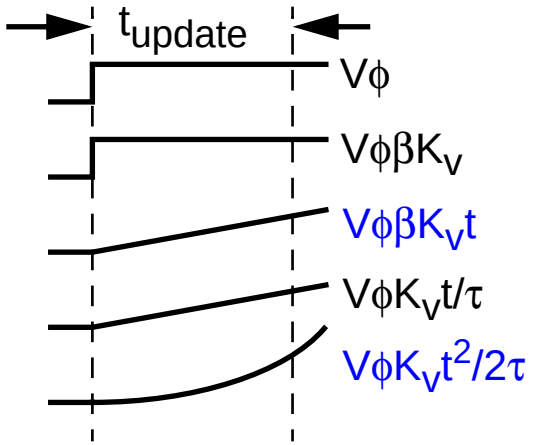
- Phase detector average duty cycle C, given by $\left(\frac{1}{2} + \frac{\Delta f}{(2 \cdot f_{bb})}\right)$ (proportional to Δf).

Observations

- Jitter generation, Jitter transfer bandwidth, Jitter tolerance and frequency lock range are all inconveniently controlled by one parameter, f_{bb}.
- Phase detector average duty-cycle is proportional to frequency error.
- Strategy: Use the average duty cycle to control loop center frequency. This decouples the lock range from jitter tolerance/generation giving more design freedom.
- If the center frequency control loop is slow enough, the resulting loop behavior will be very similar to a simple first order loop, but with extended frequency lock capability.

2nd-order BB loop





pd output

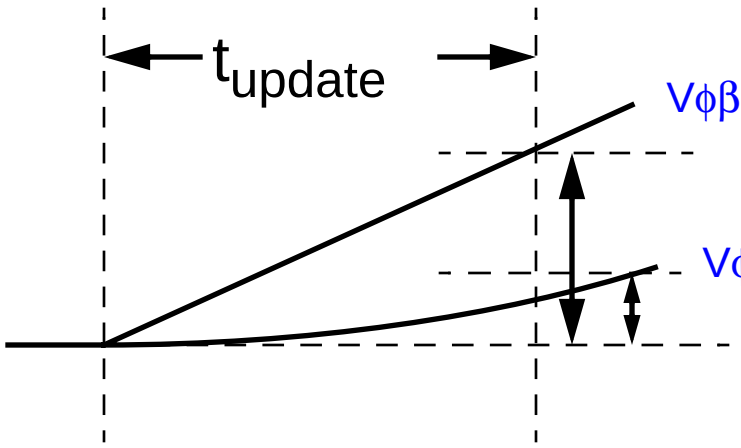
BB path frequency change

BB path phase change

Integrator path frequency change

Integrator path phase change

Stability Factor ξ



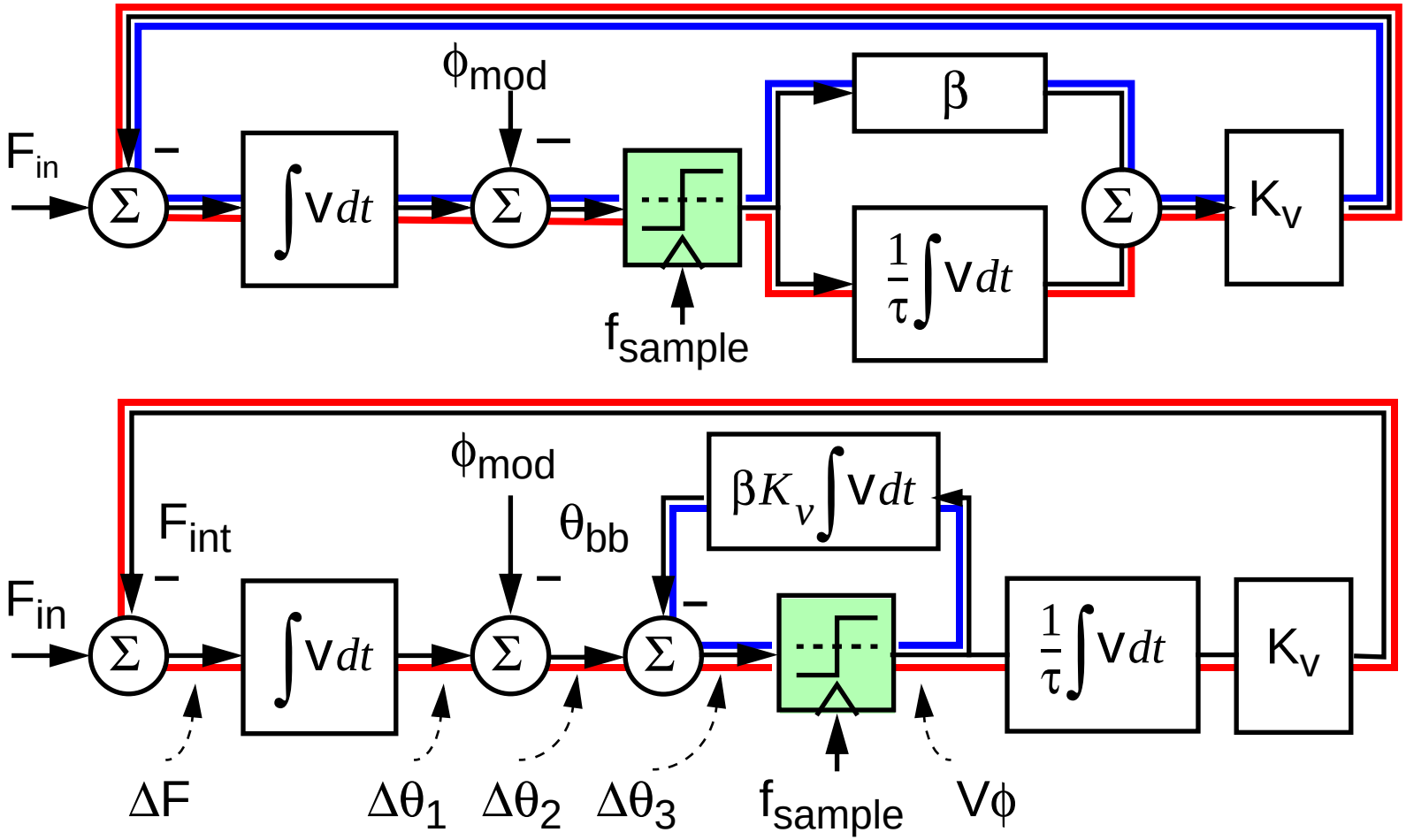
(phase change from BB path)

(phase change from integral path)

To quantify the relative independence of the two feedback loops, take ratio of phase change from BB path to the phase change of the integral path:

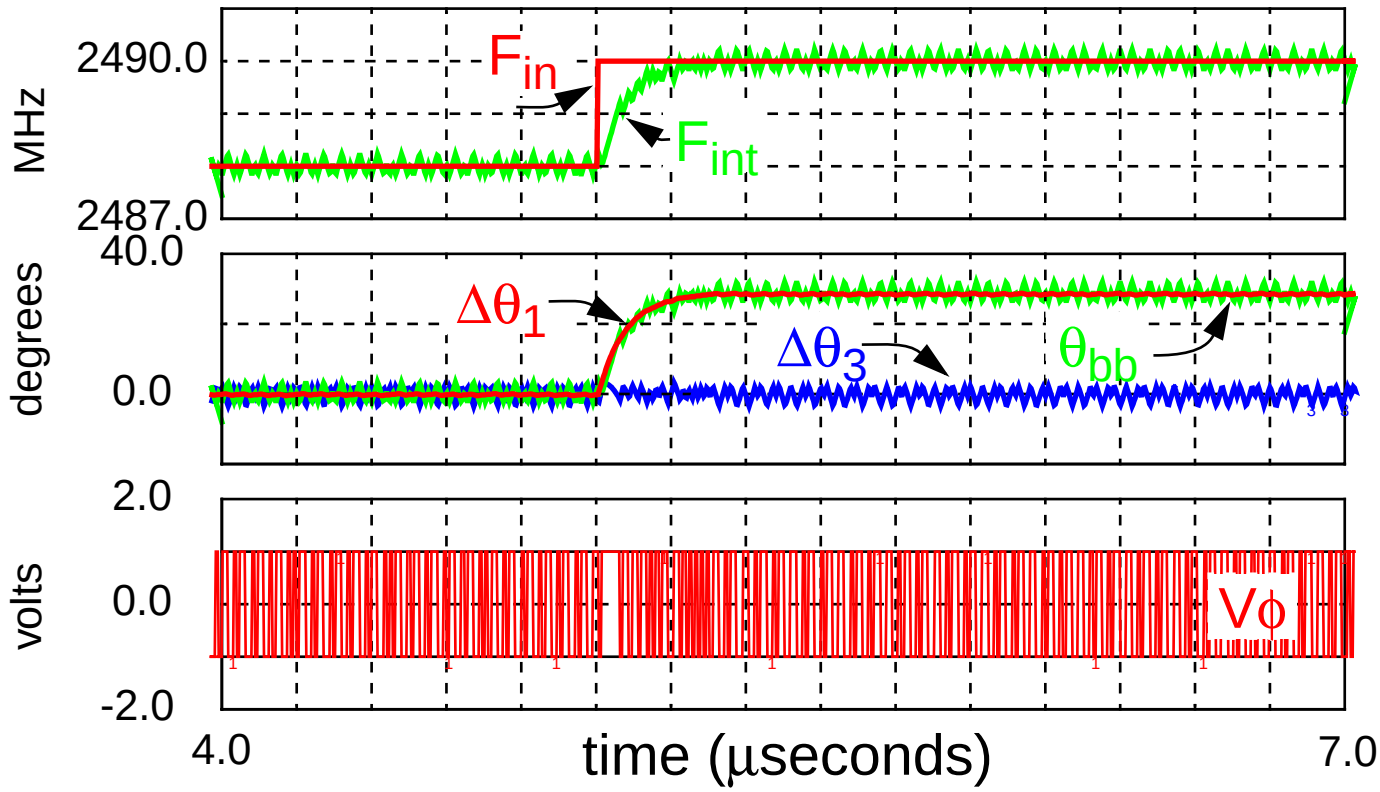
$$\xi \equiv \frac{\Delta\theta_{bb}}{\Delta\theta_{int}} = \left.\frac{\beta V_\phi K_v t}{V_\phi K_v t^2/(2\tau)}\right|_{t = t_{update}} = \frac{2\beta\tau}{t_{update}}$$

redrawing the 2nd-order loop



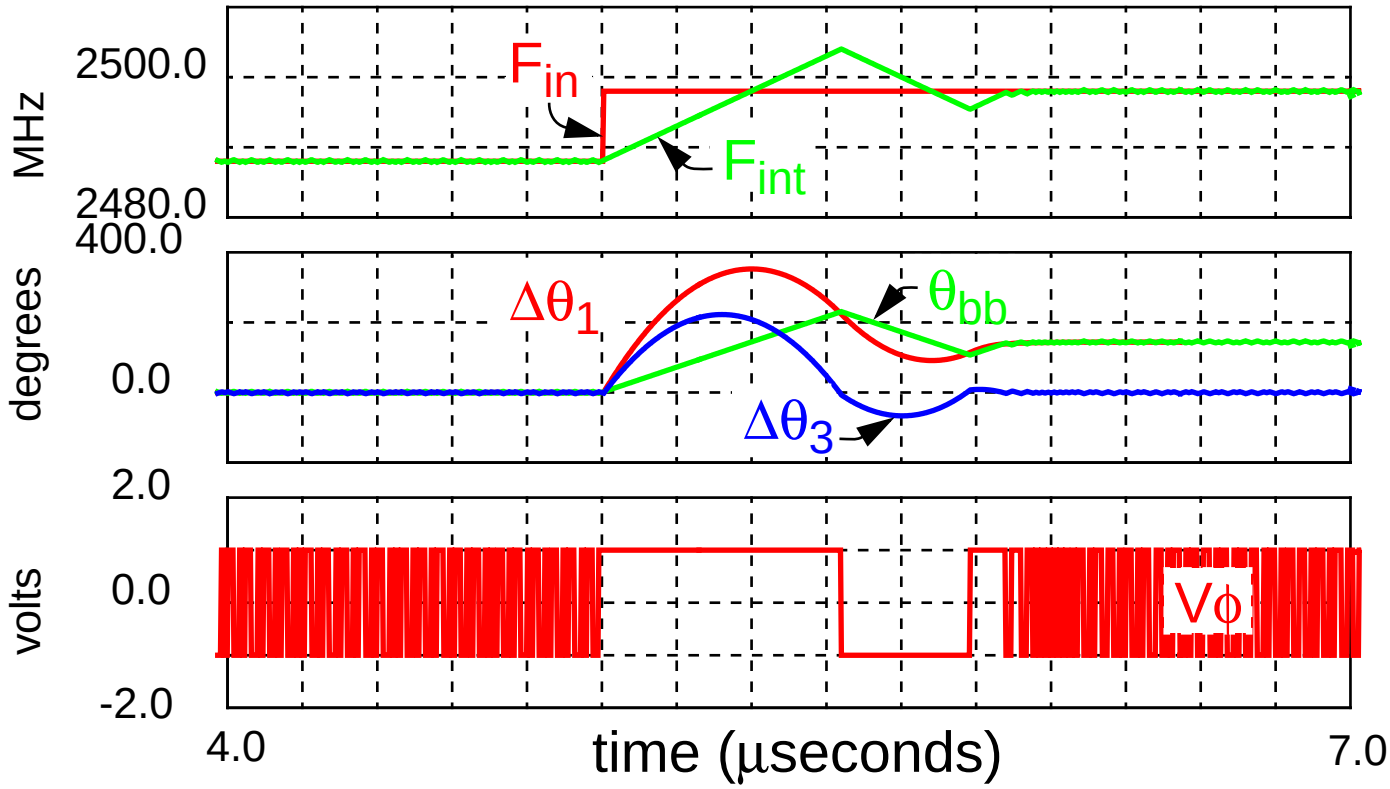
Noticing that $V\phi$ is proportional to ΔF, the system can be transformed into an inner first order bb-loop PLL (in blue) surrounded by an outer low-bandwidth frequency tracking loop (in red).

2nd-order loop: small step in F



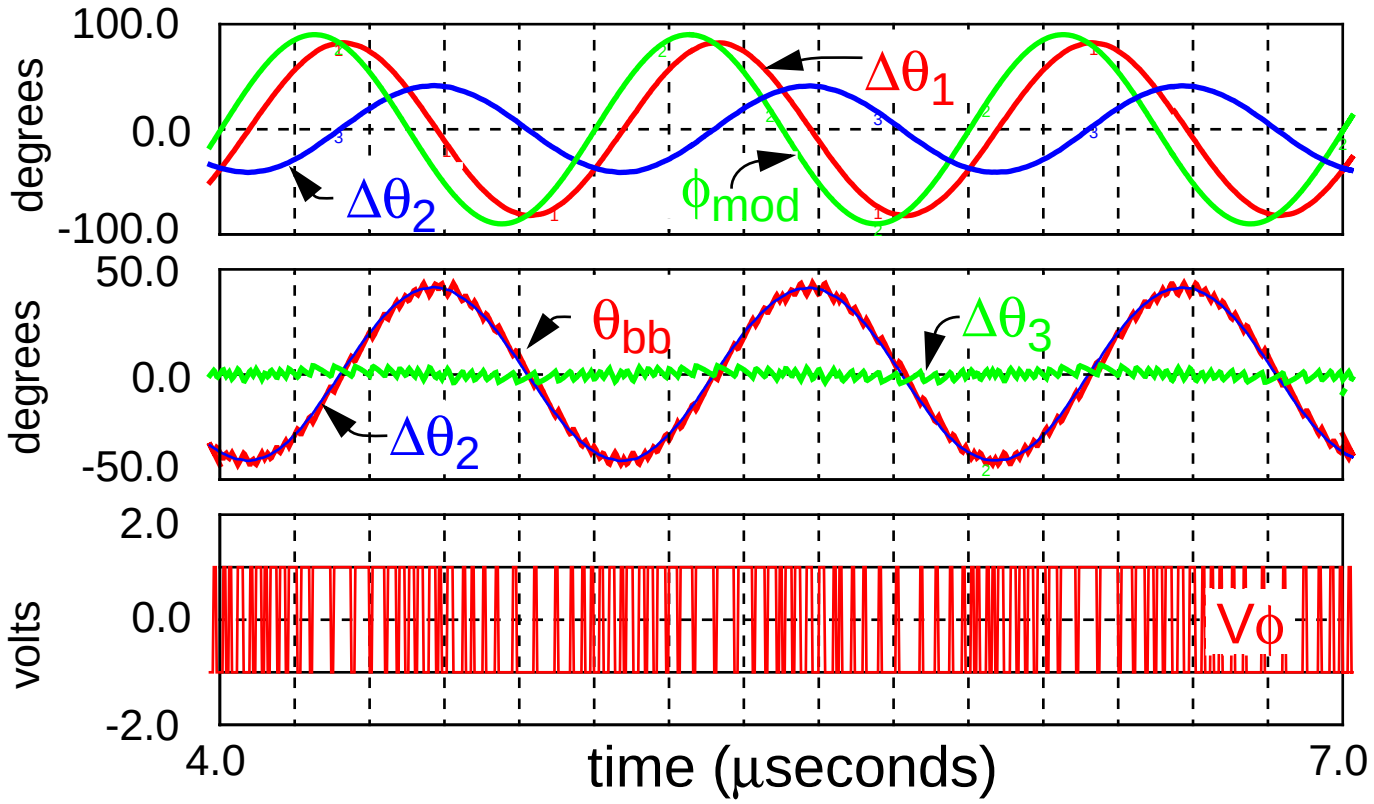
A step change in input frequency F_{in} produces a slow response F_{int} in the outer, integral loop. The resulting phase error $\Delta\theta_1$ is tracked by the inner bang-bang loop θ_{bb} to produce the final sampler phase error $\Delta\theta_3$. Notice that, unlike a linear PLL, there is no jitter accumulation at the sampler.

2nd-order loop: large step in F



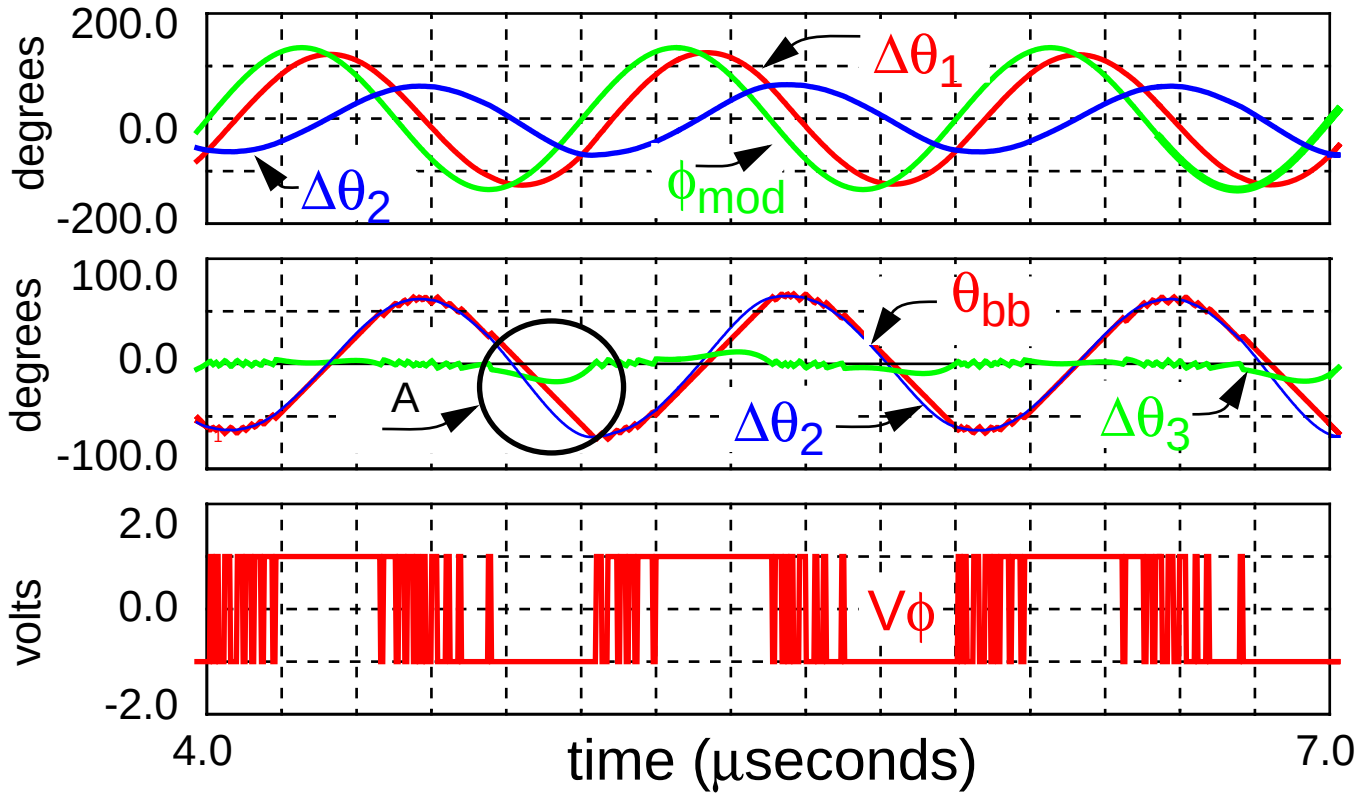
In this simulation, the input frequency step is bigger than f_{bb}, so the loop goes into slew rate limiting, leading to a transient phase error $\Delta\theta_3$ at the sampler. A fancier loop could detect slew rate limiting by the lack of PD transitions, and adaptively increase the loop frequency step size.

2nd-order loop: phase jitter tracking



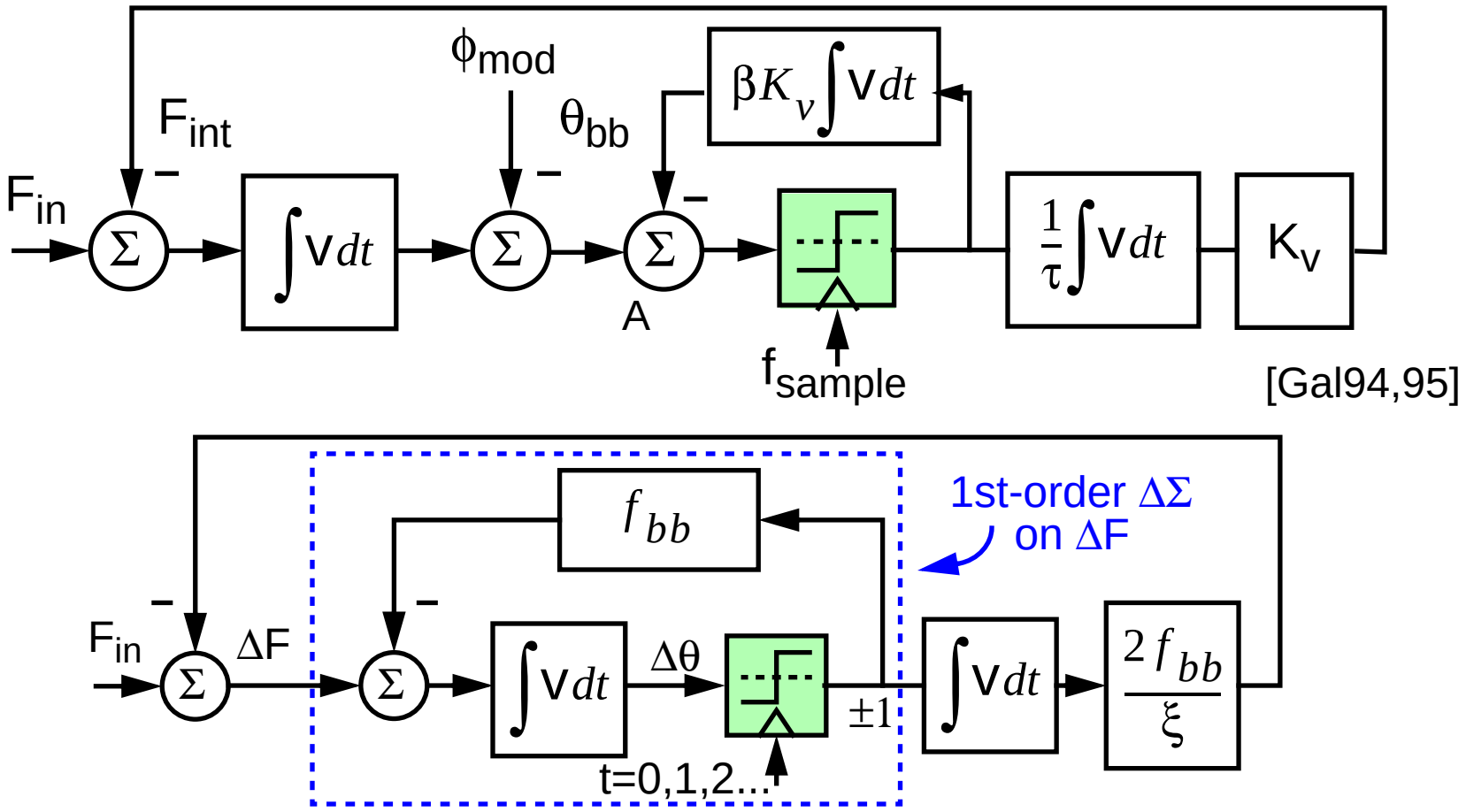
Sinusoidal phase jitter ϕ_{mod} is tracked at $\Delta\theta 1$ with a phase lag by the outer, integral loop. The resulting phase error $\Delta\theta_2$ is tracked by the inner bang-bang loop θ_{bb} to produce the final sampler phase error $\Delta\theta_3$. The PD output $V\phi$ varies with the slope of $\Delta\theta_2$ which is proportional to the instantaneous frequency error of the outer loop.

2nd-order loop: slope overload



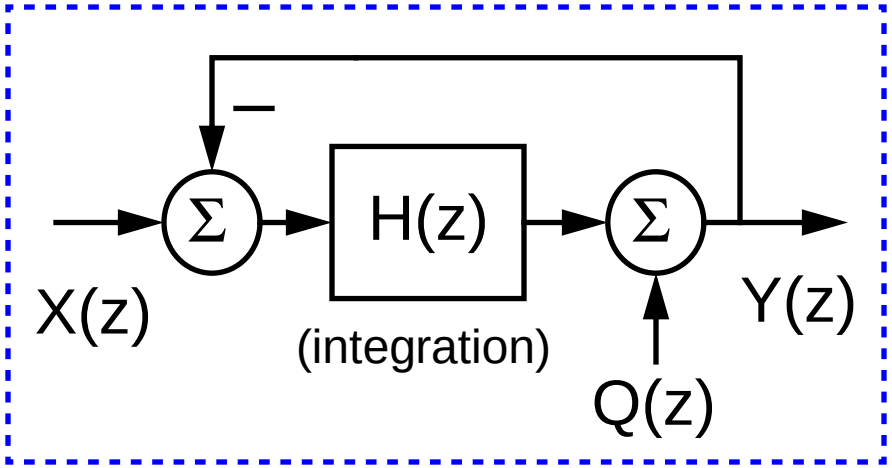
The phase modulation is increased until the instantaneous frequency error exceeds the inner loop's ability to track. Slew-rate limiting at point "A" in the inner loop θ_{bb} produces a tracking error at the sampler $\Delta\theta_3$. The loop is designed so that this situation never occurs under normal jitter tolerance conditions.

redrawing the 2nd-order loop (again)



Transform the loop by pulling the integrators through the summing node “A”. Normalize update interval to 1. Let $\beta K_v V\phi = f_{bb}$ Substitute in definition for stability factor ξ. Notice that structure in blue box is a 1st order $\Delta\Sigma$ on ΔF.

$\Delta\Sigma$ linear system analogy for bb-loop

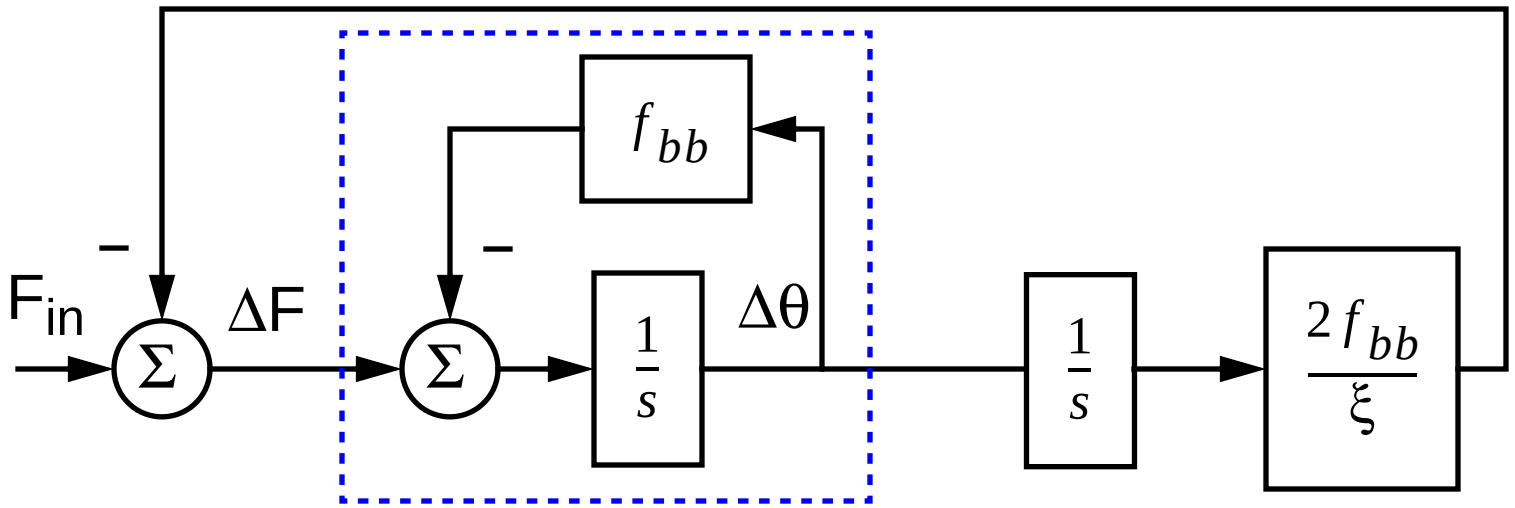


[Hau91b]

[Gal95]

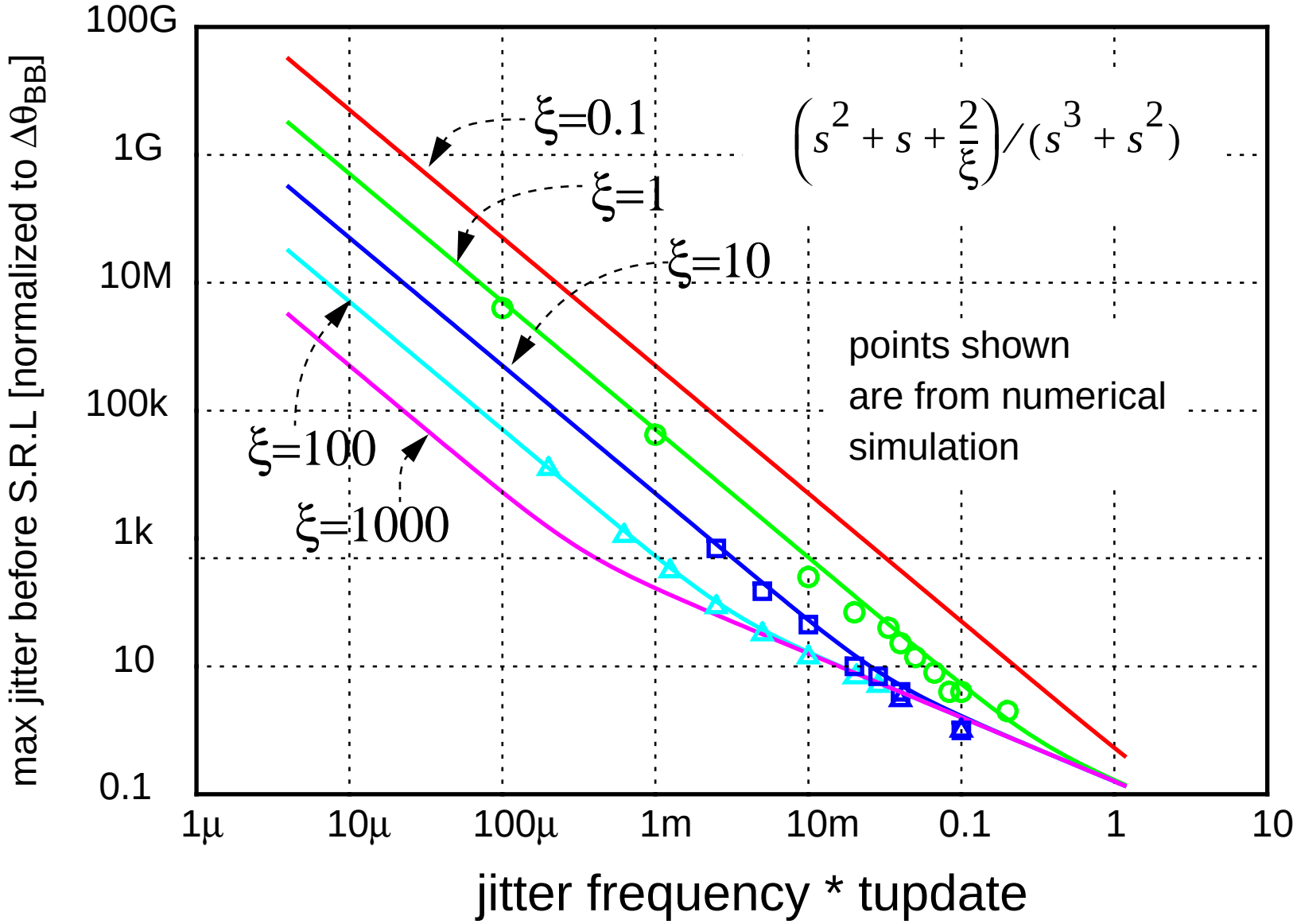
$$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}Q(z)$$

solve for slope overload



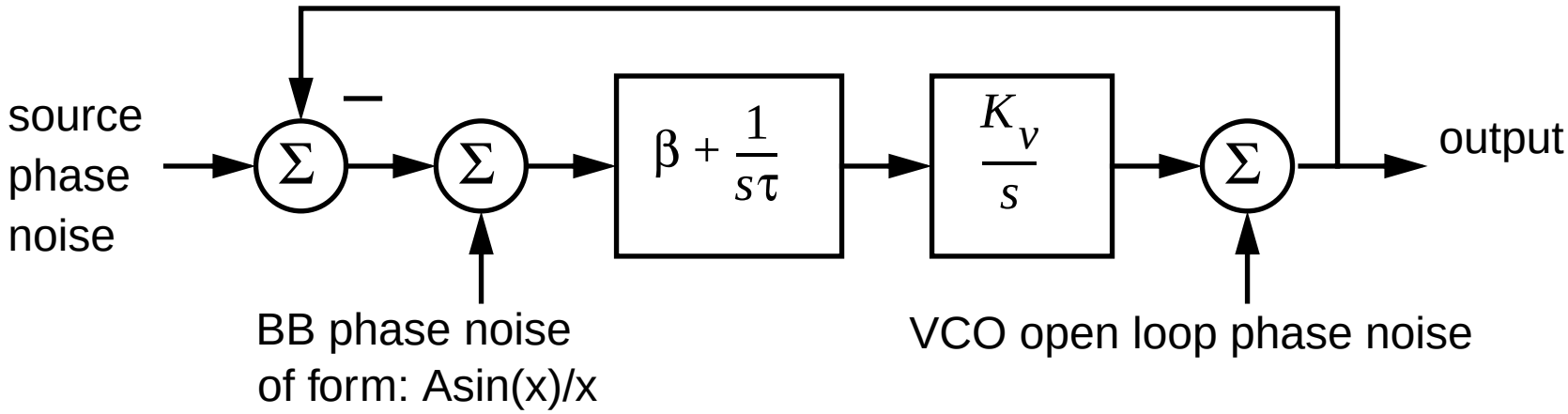
- Slew rate limiting occurs when $|\Delta F| > f_{bb}$
- Maximum input phase modulation in UI, normalized to $\Delta\theta_{bb}$ is $\left(s^2 + s + \frac{2}{\xi}\right) / (s^3 + s^2)$.
- Can be used to compute jitter tolerance.

slope overload limit vs ξ



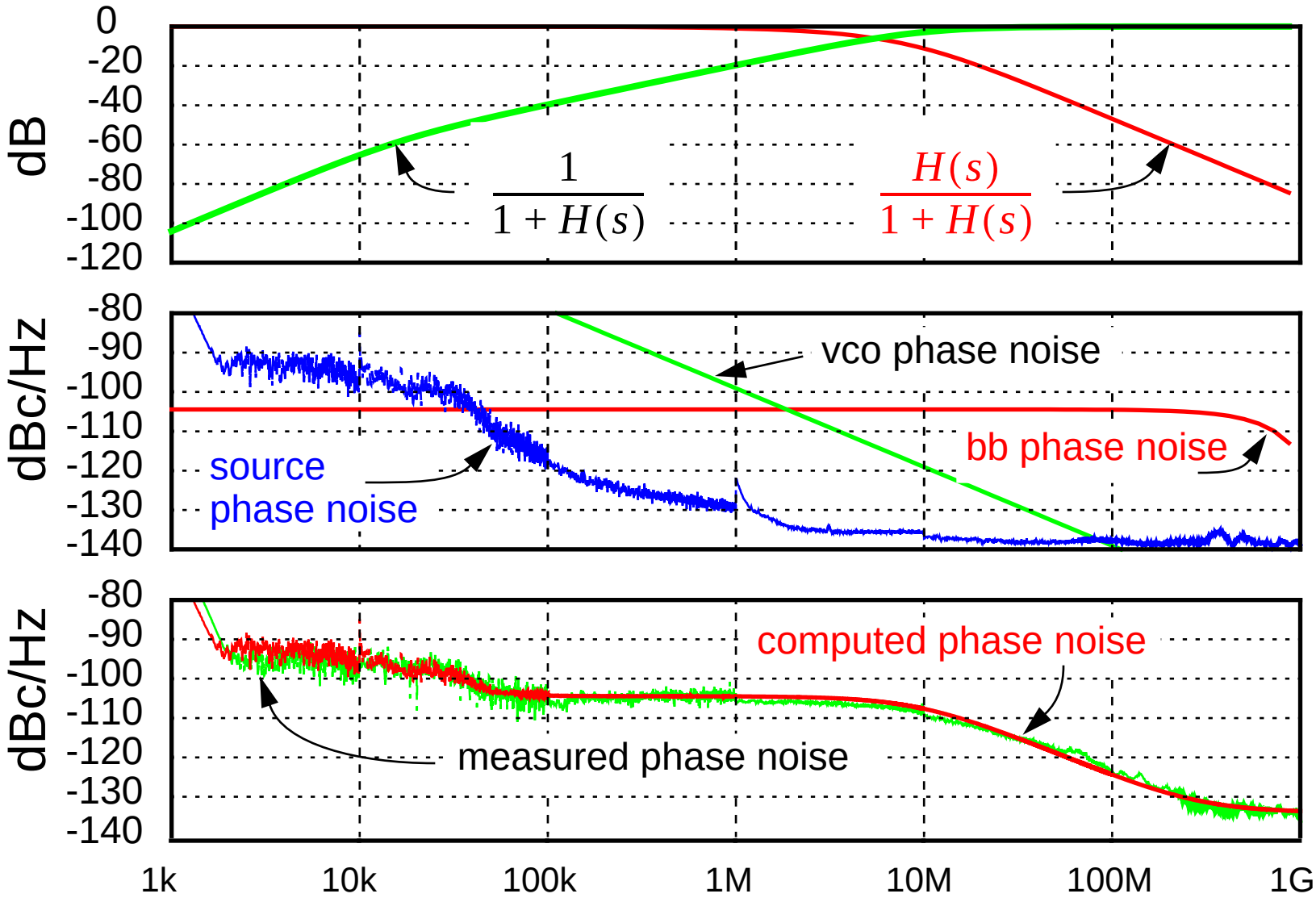
jitter generation in frequency-domain

- $\Delta\Sigma$ approximation justifies replacing BB phase detector with a noise source.
- Combine total loop phase noise by combining each phase noise source in RMS fashion.



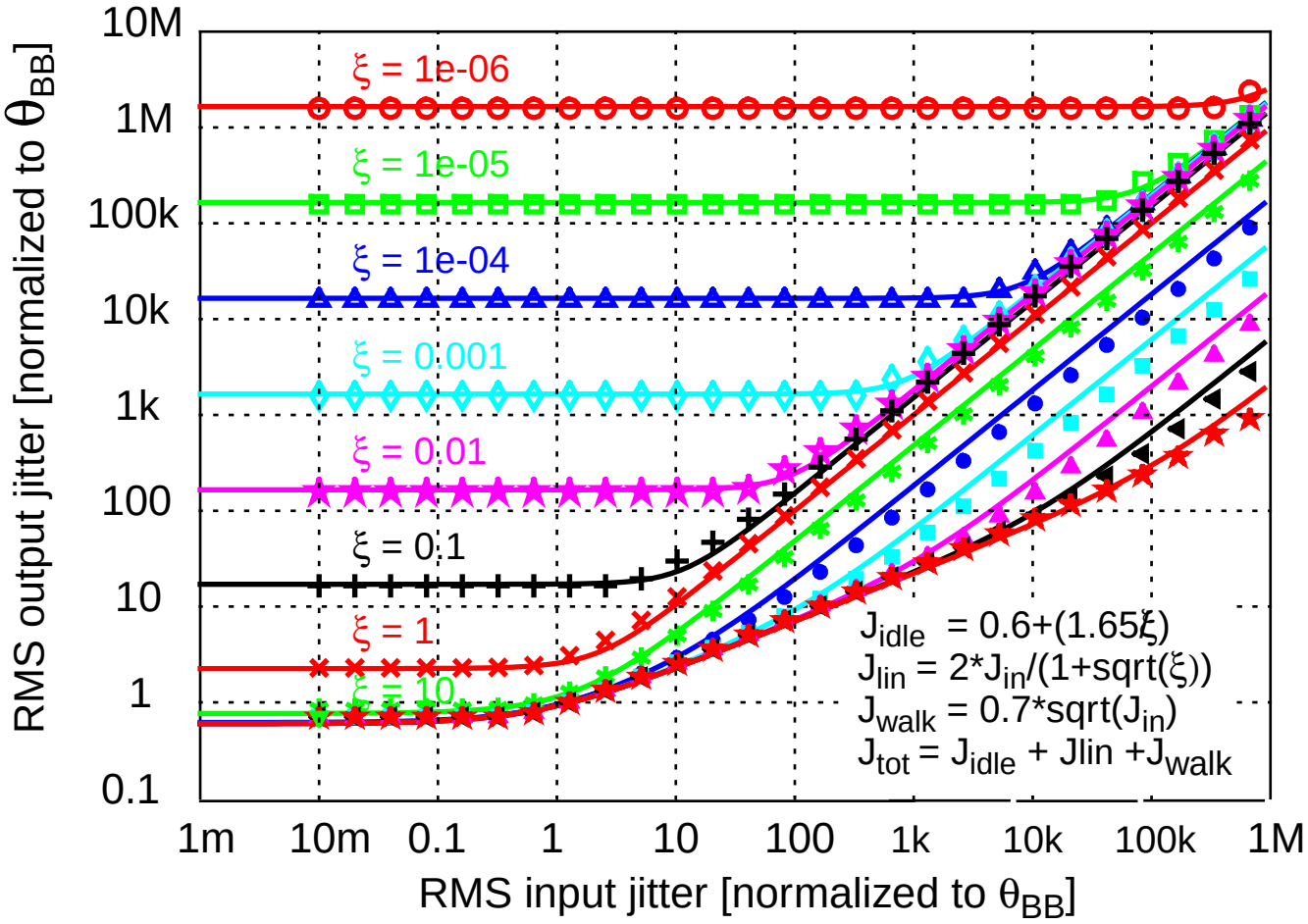
$$H(s) = \frac{K_v}{s}\left(\beta + \frac{1}{s\tau}\right)$$

example jitter generation calculation



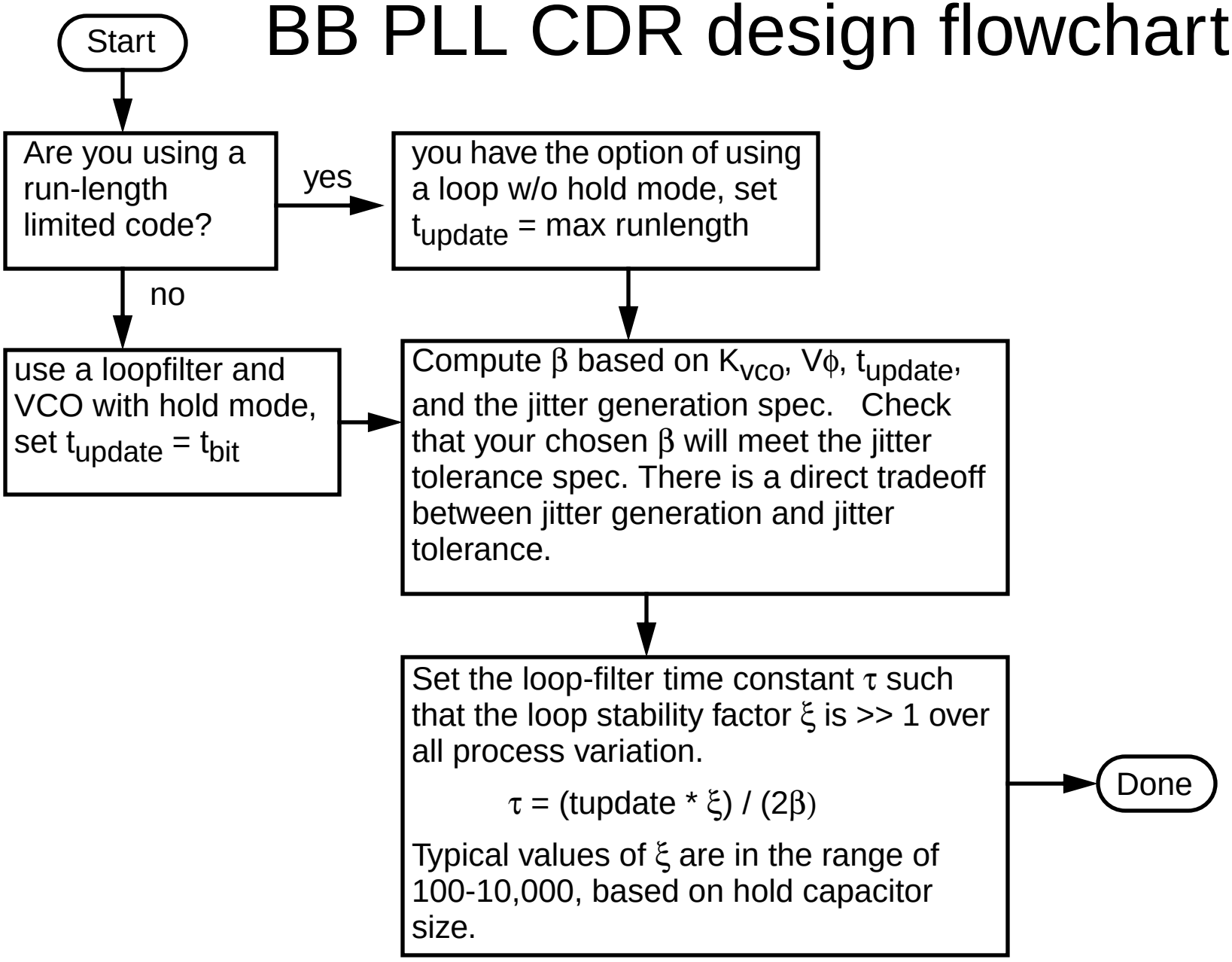
see [WSY97]: fvco=2.488 GHz, fbb = 6 MHz, ξ=32000, tupdate=400ps.

gaussian jitter generation & gain vs ξ



Simulation is for a non-tristated loop, $p_{transition}$ = 100%, with 10^8 timesteps per point. High stability-factor loops have RMS output jitter equal to the square root of the input jitter!

BB PLL CDR design flowchart



Summary

A lot of complexity for a “simple” system...

It’s more of an art than a science

After understanding:

- the components,
- the block diagrams,
- the problems and the attempted solutions,
- and the unique needs for your application,

you’ll be well equipped to craft an artful solution.

References

Clock and data recovery is a complex field. Any single presentation can only act as an introduction to the field. This eclectic collection of serial data communication references includes papers on signal degradation mechanisms, jitter measurement, phase locked loop design, simulation techniques, multiplexers and demultiplexers, and coding theory.

Every new application comes with a unique set of constraints and requirements, requiring an artful combination of techniques to be optimally addressed. I can't recommend anything better to the newcomer to this field than to read through the literature and internalize the many different techniques that exist.

Keywords appear in curly braces {}. Papers in **Boldface** appear on the short course CDROM in PDF format.

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