CDR Design Checklist

RCW 01/15/97, updated 9/18/98

1) Eye Margin

- how much noise can be added to input while maintaining target BER? (voltage margin)
- How far can clock phase alignment be varied while maintaining target BER? phase margin)
- how does the static phase error vary versus frequency, temperature and process variation?
- Is input amplifier gain, noise and offset sufficient?

2) Jitter Characteristics

- what is the jitter generation? (VCO phase noise, etc.)
- what is the jitter transfer function? (peaking and bandwidth)
- what is the jitter tracking tolerance versus frequency?

3) Pattern Dependency

- how do long runlengths affect system performance?
- is bandwidth sufficient for individual isolated bit pulses?
- are there other problematic data patterns? (resonances)
- does PLL bandwidth, jitter, and stability change versus transition density?

4) Acquisition Time

- what is the initial, power-on lock time?
- what is the phase-lock acquisition time when input source is changed?

5) How is precision achieved?

- are external capacitors, inductors needed?
- does the CDR need an external reference frequency?
- are laser-trimming or highly precise IC processes required?

6) Input/output impedance

- Is S11/S22 (input/output impedance) maintained across the frequency band?
- are reflections large enough to lead to eye closure and pattern dependency?
- is >15 dB return loss maintained across the band?

7) Power Supply

- does the CDR create power supply noise?
- how sensitive is the CDR to supply noise?
- Is the VCO self-modulated through its own supply noise? (can be “deadly”)
- what is the total static power dissipation?
- what is the die temperature under worse case conditions?

8) False lock susceptibility

- can false lock occur with particular data patterns?
- are false lock conditions be detected and eliminated?
- does the phase detector have VCO frequency leakage that can cause injection locking?
- can the VCO run faster than the phase/frequency detector can operate? (another “killer”)
- have all latchup/deadly embrace conditions been considered and eliminated?

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- how does the static phase error vary versus frequency, temperature and process variation?
- Is input amplifier gain, noise and offset sufficient?

2) Jitter Characteristics

- what is the jitter generation? (VCO phase noise, etc.)
- what is the jitter transfer function? (peaking and bandwidth)
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3) Pattern Dependency

- how do long runlengths affect system performance?
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- are there other problematic data patterns? (resonances)
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4) Acquisition Time

- what is the initial, power-on lock time?
- what is the phase-lock acquisition time when input source is changed?

5) How is precision achieved?

- are external capacitors, inductors needed?
- does the CDR need an external reference frequency?
- are laser-trimming or highly precise IC processes required?

6) Input/output impedance

- Is S11/S22 (input/output impedance) maintained across the frequency band?
- are reflections large enough to lead to eye closure and pattern dependency?
- is >15 dB return loss maintained across the band?

7) Power Supply

- does the CDR create power supply noise?
- how sensitive is the CDR to supply noise?
- Is the VCO self-modulated through its own supply noise? (can be “deadly”)
- what is the total static power dissipation?
- what is the die temperature under worse case conditions?

8) False lock susceptibility

- can false lock occur with particular data patterns?
- are false lock conditions be detected and eliminated?
- does the phase detector have VCO frequency leakage that can cause injection locking?
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CDR Design Checklist

RCW 01/15/97, updated 9/18/98

1) Eye Margin

- how much noise can be added to input while maintaining target BER? (voltage margin)
- How far can clock phase alignment be varied while maintaining target BER? phase margin)
- how does the static phase error vary versus frequency, temperature and process variation?
- Is input amplifier gain, noise and offset sufficient?

2) Jitter Characteristics

- what is the jitter generation? (VCO phase noise, etc.)
- what is the jitter transfer function? (peaking and bandwidth)
- what is the jitter tracking tolerance versus frequency?

3) Pattern Dependency

- how do long runlengths affect system performance?
- is bandwidth sufficient for individual isolated bit pulses?
- are there other problematic data patterns? (resonances)
- does PLL bandwidth, jitter, and stability change versus transition density?

4) Acquisition Time

- what is the initial, power-on lock time?
- what is the phase-lock acquisition time when input source is changed?

5) How is precision achieved?

- are external capacitors, inductors needed?
- does the CDR need an external reference frequency?
- are laser-trimming or highly precise IC processes required?

6) Input/output impedance

- Is S11/S22 (input/output impedance) maintained across the frequency band?
- are reflections large enough to lead to eye closure and pattern dependency?
- is >15 dB return loss maintained across the band?

7) Power Supply

- does the CDR create power supply noise?
- how sensitive is the CDR to supply noise?
- Is the VCO self-modulated through its own supply noise? (can be “deadly”)
- what is the total static power dissipation?
- what is the die temperature under worse case conditions?

8) False lock susceptibility

- can false lock occur with particular data patterns?
- are false lock conditions be detected and eliminated?
- does the phase detector have VCO frequency leakage that can cause injection locking?
- can the VCO run faster than the phase/frequency detector can operate? (another “killer”)
- have all latchup/deadly embrace conditions been considered and eliminated?

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